# BLS7G2729L-350P; BLS7G2729LS-350P LDMOS S-band radar power transistor Rev. 6 – 1 September 2015



#### **Product profile** 1.

### 1.1 General description

350 W LDMOS power transistor for S-band radar applications in the frequency range from 2.7 GHz to 2.9 GHz.

#### Table 1. **Typical performance**

Typical RF performance at  $T_{case} = 25$  °C;  $t_p = 300 \ \mu s$ ;  $\delta = 10$  %;  $I_{Da} = 200 \ mA$ ; in a class-AB production test circuit.

Test signal	f	V <sub>DS</sub>	PL	G <sub>p</sub>	η <sub>D</sub>	t <sub>r</sub>	t <sub>f</sub>
	(GHz)	(V)	(W)	(dB)	(%)	(ns)	(ns)
pulsed RF	2.7 to 2.9	32	350	13	50	8	5

### 1.2 Features and benefits

- High efficiency
- Excellent ruggedness
- Designed for S-band operation (2.7 GHz to 2.9 GHz)
- Excellent thermal stability
- Easy power control
- Integrated ESD protection
- High flexibility with respect to pulse formats
- Internally matched for ease of use
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

### 1.3 Applications

S-band radar applications in the frequent range 2.7 GHz to 2.9 GHz

AMPLEON

# BLS7G2729L(S)-350P

LDMOS S-band radar power transistor

### 2. Pinning information

Pin	Description	Simplified outline	Graphic symbol
BLS7G2	729L-350P (SOT539A)		
1	drain1		
2	drain2		
3	gate1		
4	gate2	3 4	3 - 5
5	source	[1]	
			<b>'F</b>
			2 sym117
BLS7G2	729LS-350P (SOT539B)		
1	drain1		
2	drain2		1
3	gate1	5	
4	gate2		3 5
5	source	[1]	
			<sup>1</sup> i
			2

[1] Connected to flange.

### 3. Ordering information

#### Table 3. Ordering information

Type number Package				
	Name	Description	Version	
BLS7G2729L-350P	-	flanged balanced ceramic package; 2 mounting holes; 4 leads	SOT539A	
BLS7G2729LS-350P	-	earless flanged balanced ceramic package; 4 leads	SOT539B	

# 4. Limiting values

#### Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Min	Max	Unit
V <sub>DS</sub>	drain-source voltage	-	65	V
V <sub>GS</sub>	gate-source voltage	-0.5	+11	V
T <sub>stg</sub>	storage temperature	-65	+150	°C
Tj	junction temperature [1]	-	225	°C

[1] Continuous use at maximum temperature will affect the reliability. For details refer to the on-line MTF calculator.

# 5. Thermal characteristics

Table 5.	Thermal characteristics			
Symbol	Parameter	Conditions	Тур	Unit
Z <sub>th(j-mb)</sub>	transient thermal impedance from junction	$T_{case}$ = 85 °C; P <sub>L</sub> = 350 W		
	to mounting base	t <sub>p</sub> = 100 μs; δ = 10 %	0.07	K/W
		t <sub>p</sub> = 200 μs; δ = 10 %	0.09	K/W
		t <sub>p</sub> = 300 μs; δ = 10 %	0.10	K/W
		t <sub>p</sub> = 100 μs; δ = 20 %	0.09	K/W

# 6. Characteristics

#### Table 6. DC characteristics

 $T_i = 25 \ ^{\circ}C$  unless otherwise specified.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V <sub>(BR)DSS</sub>	drain-source breakdown voltage	V <sub>GS</sub> = 0 V; I <sub>D</sub> = 2.2 mA	65	-	-	V
V <sub>GS(th)</sub>	gate-source threshold voltage	V <sub>DS</sub> = 10 V; I <sub>D</sub> = 220 mA	1.5	1.9	2.3	V
I <sub>DSS</sub>	drain leakage current	V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 28 V	-	-	2.8	μA
I <sub>DSX</sub>	drain cut-off current	$\label{eq:VGS} \begin{array}{l} V_{\mathrm{GS}} = V_{\mathrm{GS}(\mathrm{th})} + 3.75 \ V; \\ V_{\mathrm{DS}} = 10 \ V \end{array}$	-	39	-	A
I <sub>GSS</sub>	gate leakage current	V <sub>GS</sub> = 11 V; V <sub>DS</sub> = 0 V	-	-	280	nA
g <sub>fs</sub>	forward transconductance	V <sub>DS</sub> = 10 V; I <sub>D</sub> = 11.0 A	-	16.2	-	S
R <sub>DS(on)</sub>	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75 V;$ $I_D = 7.7 A$	-	0.065	-	Ω

#### Table 7. RF characteristics

Test signal: pulsed RF;  $t_p = 300 \ \mu s$ ;  $\delta = 10 \ \%$ ; RF performance at  $V_{DS} = 32 \ V$ ;  $I_{Dq} = 200 \ mA$ ;  $T_{case} = 25 \ ^{\circ}C$ ; unless otherwise specified, in a class-AB production circuit.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
G <sub>p</sub>	power gain	P <sub>L</sub> = 350 W	11	13	-	dB
RL <sub>in</sub>	input return loss	P <sub>L</sub> = 350 W	-	-10	-	dB
η <sub>D</sub>	drain efficiency	P <sub>L</sub> = 350 W	46	50	-	%
P <sub>droop(pulse)</sub>	pulse droop power	P <sub>L</sub> = 350 W	-	0	0.5	dB
t <sub>r</sub>	rise time	P <sub>L</sub> = 350 W	-	8	50	ns
t <sub>f</sub>	fall time	P <sub>L</sub> = 350 W	-	5	50	ns

# 7. Test information

### 7.1 Ruggedness in class-AB operation

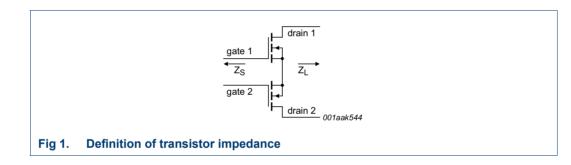
The BLS7G2729L-350P and BLS7G2729LS-350P are capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions:  $V_{DS}$  = 32 V;  $I_{Dq}$  = 200 mA;  $P_L$  = 350 W;  $t_p$  = 300 µs;  $\delta$  = 10 %.

### 7.2 Impedance information

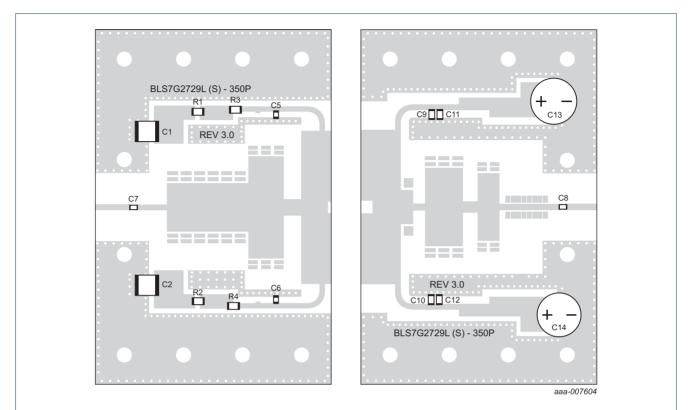
Table 6. Typical impedance	Table	8.	<b>Typical</b>	impedance
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f	Z <sub>S</sub> [1]	Z <sub>L</sub> [1]
GHz	Ω	Ω
2.7	2.8 – j8.7	1.8 – j5.1
2.8	3.9 – j8.2	2.1 – j5.4
2.9	4.8 – j9.3	1.5 – j5.7

[1] Impedances are taken at a single halve of the push-pull transistor



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### 7.3 Test circuit information

Printed-Circuit Board (PCB): Rogers RO6006;  $\varepsilon_r$  = 6.45 F/m; thickness = 0.635 mm; thickness copper plating = 35  $\mu$ m. The vias can be used as a reference to place components.

The above layout shows the test circuit used to measure the devices in production. A more appropriate application demonstration for specific customer needs can be provided. See Table 9 for list of components.

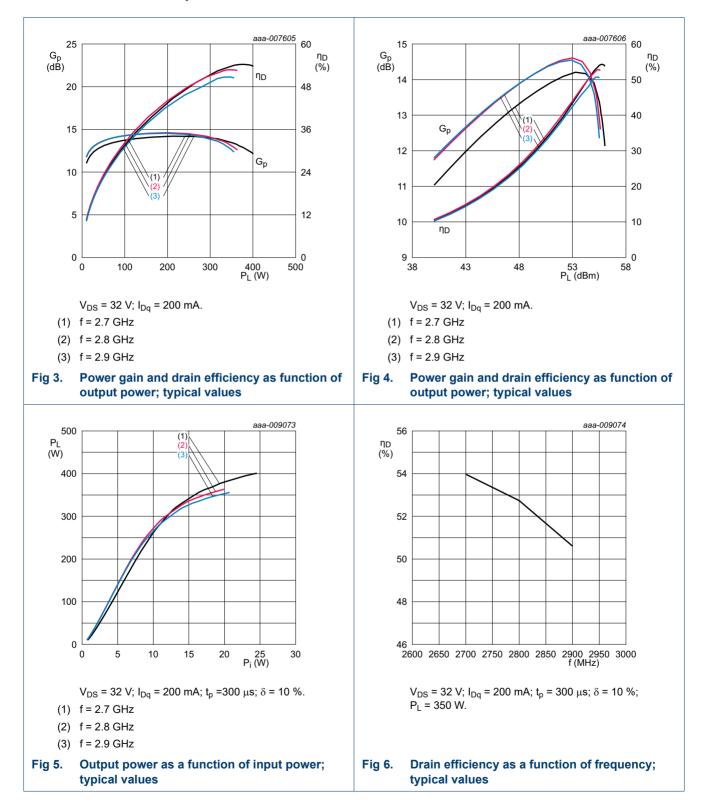
#### Fig 2. Component layout

# Table 9.List of componentsSee Figure 2 for component layout.

<u></u> ,,					
Component	Description	Value	Remarks		
C1, C2	SMD capacitor	4.7 μF, 50 V			
C5, C6	multilayer ceramic chip capacitor	12 pF	ATC800A		
C7, C8	multilayer ceramic chip capacitor	20 pF	ATC800A		
C9, C10	multilayer ceramic chip capacitor	12 pF	ATC800A		
C11, C12	multilayer ceramic chip capacitor	1 nF	ATC700A		
C13, C14	electrolytic capacitor	220 μF, 63 V			
R1, R2	SMD resistor	9.1 Ω	SMD 0805		
R3, R4	SMD resistor	8 Ω	SMD 0805		

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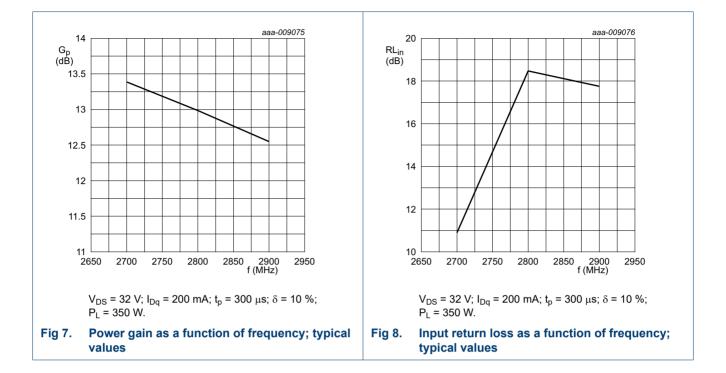


### 7.4 Graphical data

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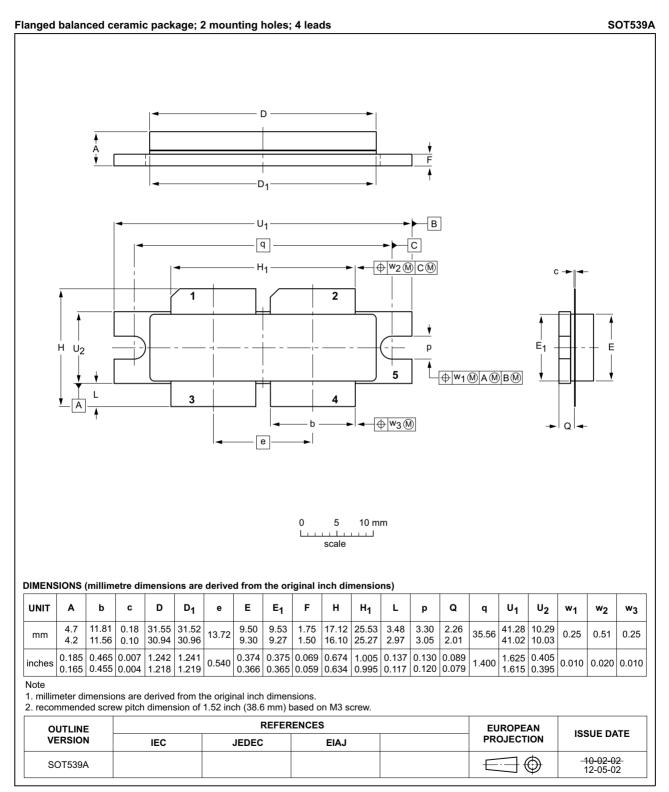


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Product data sheet

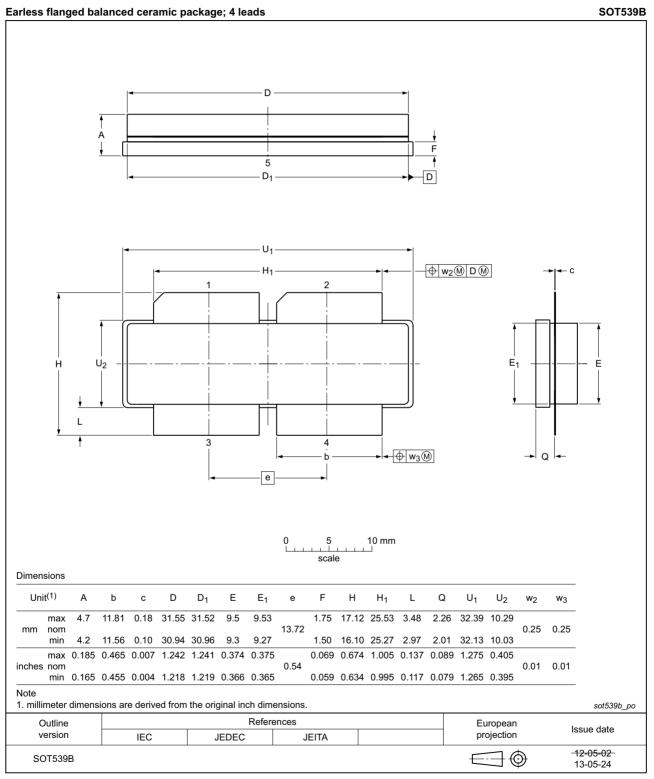
### LDMOS S-band radar power transistor

# 8. Package outline



### Fig 9. Package outline SOT539A

### LDMOS S-band radar power transistor



### Fig 10. Package outline SOT539B

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# 9. Handling information

#### CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the ANSI/ESD S20.20, IEC/ST 61340-5, JESD625-A or equivalent standards.

# 10. Abbreviations

Table 10. Abbreviations				
Acronym	Description			
ESD	ElectroStatic Discharge			
LDMOS	Laterally Diffused Metal-Oxide Semiconductor			
MTF	Median Time to Failure			
S-band	Short wave Band			
SMD	Surface-Mounted Device			
VSWR	Voltage Standing-Wave Ratio			

# 11. Revision history

### Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes	
BLS7G2729L-350P_LS-350P #6	20150901	Product data sheet		BLS7G2729L-350P_LS-350P v.5	
Modifications:	• The format of this document has been redesigned to comply with the new identity guidelines of Ampleon.				
	<ul> <li>Legal texts have been adapted to the new company name where appropriate.</li> </ul>				
BLS7G2729L-350P_LS-350P v.5	20140516	Product data sheet	-	BLS7G2729L-350P_LS-350P v.4	
BLS7G2729L-350P_LS-350P v.4	20130923	Product data sheet	-	BLS7G2729L-350P_LS-350P v.3	
BLS7G2729L-350P_LS-350P v.3	20130712	Objective data sheet	-	BLS7G2729L-350P_LS-350P v.2	
BLS7G2729L-350P_LS-350P v.2	20130506	Objective data sheet	-	BLS7G2729L-350P_LS-350P v.1	
BLS7G2729L-350P_LS-350P v.1	20110524	Objective data sheet	-	-	

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Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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