BLF8G10L-160; Power LDMOS transistor Rev. 4 — 1 September 2015

AMMPLEON Product data sheet

Product profile

1.1 General description

160 W LDMOS power transistor for base station applications at frequencies from 920 MHz to 960 MHz.

Typical performance Table 1.

Typical RF performance at $T_{case} = 25$ °C in a common source class-AB production test circuit.

Test signal	f	I _{Dq}	V _{DS}	P _{L(AV)}	Gp	η _D	ACPR
	(MHz)	(mA)	(V)	(W)	(dB)	(%)	(dBc)
2-carrier W-CDMA	920 to 960	1100	30	35	19.7	29	-38 [1]

^[1] Test signal: 3GPP; test model 1; 64 DPCH; PAR = 7.5 dB at 0.01 % probability on CCDF per carrier. Carrier spacing 5 MHz.

1.2 Features and benefits

- Excellent ruggedness
- High efficiency
- Low R_{th} providing excellent thermal stability
- Designed for broadband operation (920 MHz to 960 MHz)
- Lower output capacitance for improved performance in Doherty applications
- Designed for low memory effects providing excellent pre-distortability
- Internally matched for ease of use
- Integrated ESD protection
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

1.3 Applications

RF power amplifiers for W-CDMA base stations and multi carrier applications in the 920 MHz to 960 MHz frequency range

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
BLF8G10	L-160 (SOT502A)		
1	drain		,
2	gate	$\begin{array}{c c} & & \\ & & \\ & & \\ \end{array}$	اَـا
3	source	[1]	2
			3 sym112
BLF8G10	LS-160 (SOT502B)		
1	drain		_
2	gate	1 3	1 الله
3	source	[1]	2
			- 1 3
			sym112

^[1] Connected to flange

3. Ordering information

Table 3. Ordering information

Type number	Packag	Package				
	Name	Description	Version			
BLF8G10L-160	-	flanged LDMOST ceramic package; 2 mounting holes; 2 leads	SOT502A			
BLF8G10LS-160	-	earless flanged LDMOST ceramic package; 2 leads	SOT502B			

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	65	V
V_{GS}	gate-source voltage		-0.5	+13	V
T _{stg}	storage temperature		-65	+150	°C
Tj	junction temperature		-	200	°C

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Тур	Unit
$R_{\text{th(j-c)}}$	thermal resistance from junction to case	T_{case} = 80 °C; P_L = 35 W; V_{DS} = 30 V; I_{Dq} = 1100 mA	0.50	K/W

BLF8G10L-160_8G10LS-160#4

6. Characteristics

Table 6. Characteristics

 $T_i = 25$ °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V _{(BR)DSS}	drain-source breakdown voltage	$V_{GS} = 0 \text{ V}; I_D = 2.2 \text{ mA}$	65	-	-	V
V _{GS(th)}	gate-source threshold voltage	V_{DS} = 10 V; I_{D} = 220 mA	1.5	2.0	2.3	V
I _{DSS}	drain leakage current	$V_{GS} = 0 \text{ V}; V_{DS} = 28 \text{ V}$	-	-	5	μА
I _{DSX}	drain cut-off current	$V_{GS} = V_{GS(th)} + 3.75 \text{ V};$ $V_{DS} = 10 \text{ V}$	-	37.0	-	Α
I _{GSS}	gate leakage current	V_{GS} = 11 V; V_{DS} = 0 V	-	-	0.5	μΑ
9 _{fs}	forward transconductance	V_{DS} = 10 V; I_{D} = 7.7 A	-	14.6	-	S
R _{DS(on)}	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75 \text{ V};$ $I_D = 7.7 \text{ A}$	-	86	-	mΩ

7. Test information

Table 7. Functional test information

Test signal: 2-carrier W-CDMA; PAR = 7.5 dB at 0.01 % probability on the CCDF; 3GPP test model 1; 64 DPCH; f_1 = 920 MHz; f_2 = 925 MHz; f_3 = 955 MHz; f_4 = 960 MHz; RF performance at V_{DS} = 30 V; I_{Dq} = 1100 mA; T_{case} = 25 °C; unless otherwise specified; in a class-AB production test circuit.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
G_p	power gain	$P_{L(AV)} = 35 W$	19	19.7	-	dB
RLin	input return loss	$P_{L(AV)} = 35 W$	-	-15	-10	dB
η_{D}	drain efficiency	$P_{L(AV)} = 35 W$	27	29	-	%
ACPR	adjacent channel power ratio	$P_{L(AV)} = 35 W$	-	-38	-34	dBc

7.1 Ruggedness in class-AB operation

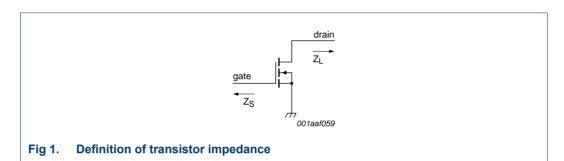
The BLF8G10L-160 and BLF8G10LS-160 are capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: $V_{DS} = 30 \text{ V}$; $I_{Dq} = 1100 \text{ mA}$; $P_L = 130 \text{ W}$ (CW); f = 920 MHz to 960 MHz.

7.2 Impedance information

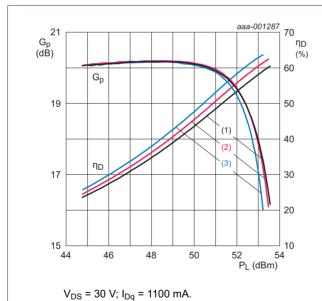
Typical impedance information I_{Da} = 1100 mA; main transistor V_{DS} = 30 V.

 $Z_{\rm S}$ and $Z_{\rm L}$ defined in Figure 1.

f	Z _S	Z _L
(MHz)	(Ω)	(Ω)
925	4.0 – j3.8	1.7 – j2.5
942	4.4 – j4.2	1.5 – j2.2
960	4.6 – j4.1	1.4 – j2.3

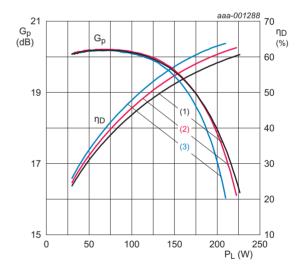


7.3 CW pulse



- (1) f = 920 MHz
- (2) f = 940 MHz
- (3) f = 960 MHz

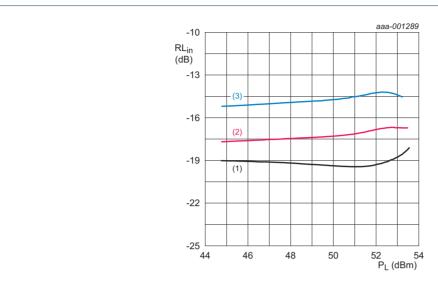
Power gain and drain efficiency as function of output power; typical values



 $V_{DS} = 30 \text{ V}; I_{Dq} = 1100 \text{ mA}.$

- (1) f = 920 MHz
- (2) f = 940 MHz
- (3) f = 960 MHz

Fig 3. Power gain and drain efficiency as function of output power; typical values

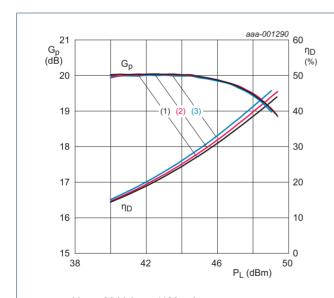


 $V_{DS} = 30 \text{ V}; I_{Dq} = 1100 \text{ mA}.$

- (1) f = 920 MHz
- (2) f = 940 MHz
- (3) f = 960 MHz

Fig 4. Input return loss as a function of output power; typical values

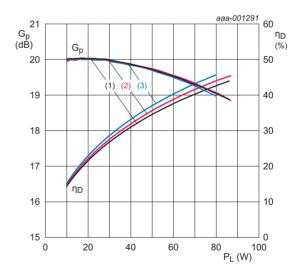
7.4 2-Carrier W-CDMA



 V_{DS} = 30 V; I_{Dq} = 1100 mA.

- (1) f = 920 MHz
- (2) f = 940 MHz
- (3) f = 960 MHz

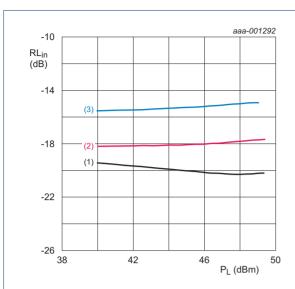
Fig 5. Power gain and drain efficiency as function of output power; typical values



 $V_{DS} = 30 \text{ V}; I_{Dq} = 1100 \text{ mA}.$

- (1) f = 920 MHz
- (2) f = 940 MHz
- (3) f = 960 MHz

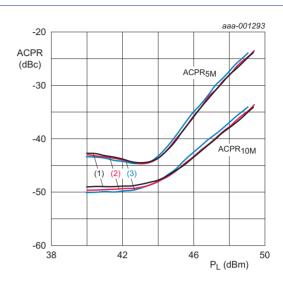
Fig 6. Power gain and drain efficiency as function of output power; typical values



$$V_{DS}$$
 = 30 V; I_{Dq} = 1100 mA.

- (1) f = 920 MHz
- (2) f = 940 MHz
- (3) f = 960 MHz

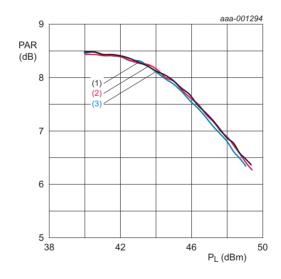
Fig 7. Input return loss as a function of output power; typical values



$$V_{DS} = 30 \text{ V}; I_{Dq} = 1100 \text{ mA}.$$

- (1) f = 920 MHz
- (2) f = 940 MHz
- (3) f = 960 MHz

Fig 8. Adjacent channel power ratio (5 MHz and 10 MHz) as function of output power; typical values

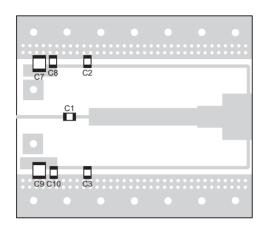


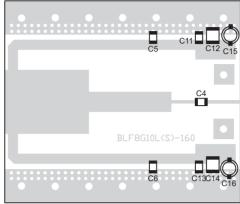
 $V_{DS} = 30 \text{ V}; I_{Dq} = 1100 \text{ mA}.$

- (1) f = 920 MHz
- (2) f = 940 MHz
- (3) f = 960 MHz

Fig 9. Peak-to-average ratio as a function of output power; typical values

7.5 Circuit





aaa-001295

Printed-Circuit Board (PCB): Rogers RO4350; ϵ_r = 3.5 F/m; thickness = 0.762 mm; thickness copper plating = 35 μ m.

The vias can be used as a reference to place components.

The above layout shows the test circuit used to measure the devices in production. A more appropriate application demonstration for specific customer needs can be provided.

See Table 9 for list of components.

Fig 10. Component layout

Table 9. List of components

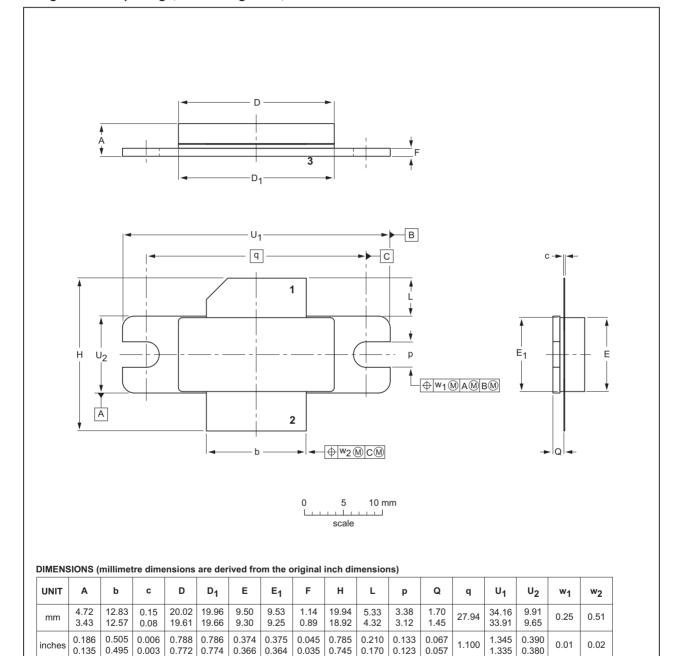
See Figure 10 for component layout.

Component	Description	Value	Remarks
C1, C2, C3, C4, C5, C6	multilayer ceramic chip capacitor	82 pF	ATC 800B
C7, C9, C12, C14	multilayer ceramic chip capacitor	10 μF	Murata
C8, C10, C11, C13	multilayer ceramic chip capacitor	1 μF	Murata
C15, C16	electrolytic capacitor	470 μF; 63 V	

8. Package outline

Flanged ceramic package; 2 mounting holes; 2 leads

SOT502A

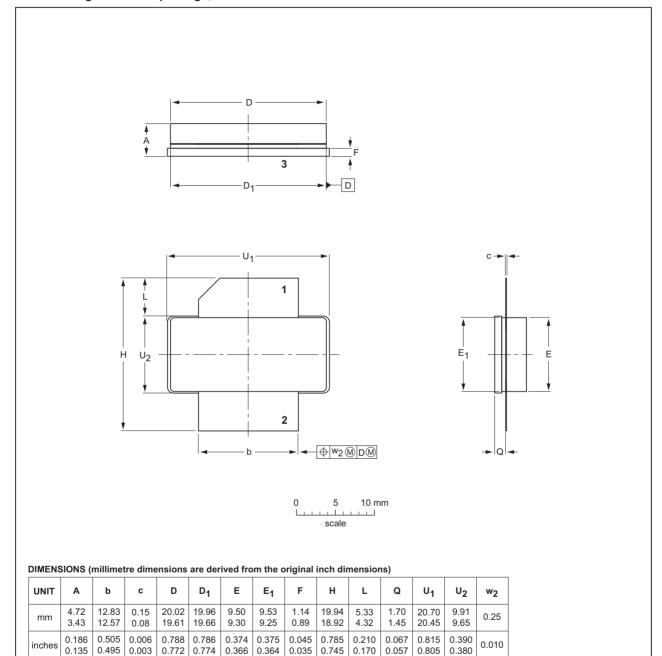


OUTLINE		REFER	RENCES	EUROPEAN	ISSUE DATE
VERSION	IEC	JEDEC	JEITA	PROJECTION	ISSUE DATE
SOT502A					-03-01-10- 12-05-02

Fig 11. Package outline SOT502A

Earless flanged ceramic package; 2 leads

SOT502B



OUTLINE		REFER	RENCES	EUROPEAN	ICCUE DATE
VERSION	IEC	JEDEC	JEITA	PROJECTION	ISSUE DATE
SOT502B					07-05-09 12-05-02

Fig 12. Package outline SOT502B

9. Abbreviations

Table 10. Abbreviations

Acronym	Description
3GPP	Third Generation Partnership Project
CCDF	Complementary Cumulative Distribution Function
CW	Continuous Wave
DPCH	Dedicated Physical CHannel
ESD	ElectroStatic Discharge
LDMOS	Laterally Diffused Metal Oxide Semiconductor
LDMOST	Laterally Diffused Metal Oxide Semiconductor Transistor
PAR	Peak-to-Average power Ratio
RF	Radio Frequency
VSWR	Voltage Standing Wave Ratio
W-CDMA	Wideband Code Division Multiple Access

10. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLF8G10L-160_8G10LS-160#4	20150901	Product data sheet	-	BLF8G10L-160_8G10LS-160 v.3
Modifications:	 The format of this document has been redesigned to comply with the new identity guidelines of Ampleon. Legal texts have been adapted to the new company name where appropriate. 			
	Legartext	s nave been adapted to t	ne new company	name where appropriate.
BLF8G10L-160_8G10LS-160 v.3	20120216	Product data sheet		BLF8G10L-160_8G10LS-160 v.2
BLF8G10L-160_8G10LS-160 v.2	20111121	Preliminary data sheet		BLF8G10L-160_8G10LS-160 v.1
BLF8G10L-160_8G10LS-160 v.1	20110519	Objective data sheet	-	-

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11.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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BLF8G10L-160; BLF8G10LS-160

Power LDMOS transistor

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Power LDMOS transistor

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