Power LDMOS transistor

Rev. 2 — 1 September 2015

AMPLEON Product data sheet

# 1. Product profile

## 1.1 General description

135 W LDMOS power transistor for industrial applications at frequencies from 700 MHz to 1000 MHz.

### Table 1.Typical performance

Typical RF performance at  $T_{case} = 25$  °C in a class-AB production test circuit.

Test signal	f	V <sub>DS</sub>	P <sub>L(AV)</sub>	G <sub>p</sub>	η <sub>D</sub>	ACPR
	(MHz)	(V)	(W)	(dB)	(%)	(dBc)
2-carrier W-CDMA	869 to 894	28	26.5	21.0	28.0	-39 <mark>[1]</mark>

[1] Test signal: 3GPP; test model 1; 64 DPCH; PAR = 7.5 dB at 0.01 % probability on CCDF per carrier; carrier spacing 5 MHz.

## 1.2 Features and benefits

- Easy power control
- Integrated ESD protection
- Enhanced ruggedness
- High efficiency
- Excellent thermal stability
- Designed for broadband operation (700 MHz to 1000 MHz)
- Internally matched for ease of use
- Compliant to Directive 2002/95/EC, regarding restriction of hazardous substances (RoHS)

## 1.3 Applications

RF power amplifiers for ISM applications in the 700 MHz to 1000 MHz frequency range

# 2. Pinning information

Pin	Description	Simplified outlin	e Graphic symbol
BLF10M6	6135 (SOT502A)	1	I
1	drain		
2	gate		、   1
3	source		3 2
BLF10M6	6LS135 (SOT502B)	ļ	
1	drain		
2	gate		1 لــــا
3	source	[ <u>1]</u> 3	2

[1] Connected to flange.

# 3. Ordering information

#### Table 3.Ordering information

Type number	Package				
	Name	Description	Version		
BLF10M6135	-	flanged ceramic package; 2 mounting holes; 2 leads	SOT502A		
BLF10M6LS135	-	earless flanged ceramic package; 2 leads	SOT502B		

## 4. Limiting values

#### Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>DS</sub>	drain-source voltage		-	65	V
V <sub>GS</sub>	gate-source voltage		-0.5	+13	V
T <sub>stg</sub>	storage temperature		-65	+150	°C
Tj	junction temperature	[1]	-	225	°C

[1] Continuous use at maximum temperature will affect reliability.

## 5. Thermal characteristics

#### Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Туре	Тур	Unit
R <sub>th(j-case)</sub>		T <sub>case</sub> = 80 °C; P <sub>L</sub> = 25 W	BLF10M6135	0.68	K/W
	junction to case		BLF10M6LS135	0.56	K/W

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## 6. Characteristics

#### Table 6.DC characteristics

 $T_i = 25 \ ^{\circ}C$  unless otherwise specified.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V <sub>(BR)DSS</sub>	drain-source breakdown voltage	V <sub>GS</sub> = 0 V; I <sub>D</sub> = 0.8 mA	65	-	-	V
V <sub>GS(th)</sub>	gate-source threshold voltage	V <sub>DS</sub> = 10 V; I <sub>D</sub> = 180 mA	1.4	1.9	2.4	V
V <sub>GSq</sub>	gate-source quiescent voltage	V <sub>DS</sub> = 28 V; I <sub>D</sub> = 950 mA	1.6	2.1	2.6	V
I <sub>DSS</sub>	drain leakage current	V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 28 V	-	-	3	μA
I <sub>DSX</sub>	drain cut-off current	$V_{GS} = V_{GS(th)} + 3.75 \text{ V};$ $V_{DS} = 10 \text{ V}$	24	32	-	A
I <sub>GSS</sub>	gate leakage current	V <sub>GS</sub> = 11 V; V <sub>DS</sub> = 0 V	-	-	300	nA
9 <sub>fs</sub>	forward transconductance	V <sub>DS</sub> = 10 V; I <sub>D</sub> = 9 A	7	13	-	S
R <sub>DS(on)</sub>	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75 V;$ $I_D = 6.3 A$	-	0.1	-	Ω

#### Table 7.AC characteristics

 $T_i = 25 \$ °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
C <sub>rs</sub>	feedback capacitance	V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 28 V; f = 1 MHz	-	2.0	-	pF

#### Table 8. RF characteristics

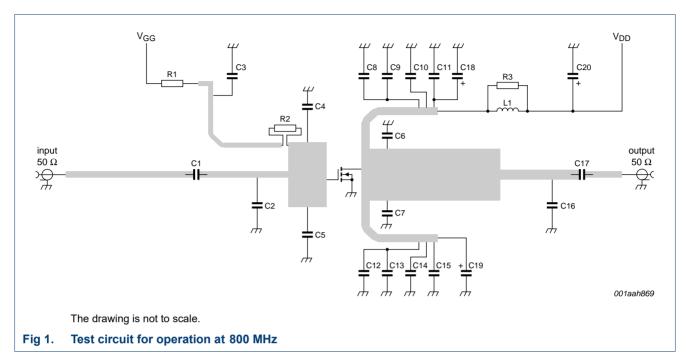
Test signal: 2-carrier W-CDMA; PAR 7.5 dB at 0.01 % probability on CCDF; 3GPP test model 1; 1-64 DPCH;  $f_1 = 871.5$  MHz;  $f_2 = 876.5$  MHz;  $f_3 = 886.5$  MHz;  $f_4 = 891.5$  MHz; RF performance at  $V_{DS} = 28$  V;  $I_{Dq} = 950$  mA;  $T_{case} = 25$  °C; unless otherwise specified; in a class-AB production test circuit.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
G <sub>p</sub>	power gain	P <sub>L(AV)</sub> = 26.5 W	20.0	21.0	-	dB
RL <sub>in</sub>	input return loss	P <sub>L(AV)</sub> = 26.5 W	-	-10.0	-6.5	dB
η <sub>D</sub>	drain efficiency	P <sub>L(AV)</sub> = 26.5 W	26.0	28.0	-	%
ACPR	adjacent channel power ratio	P <sub>L(AV)</sub> = 26.5 W	-	-39	-36.5	dBc

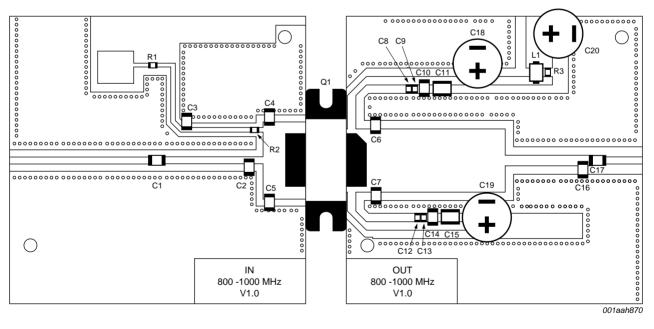
# 7. Test information

## 7.1 Ruggedness in class-AB operation

The BLF10M6135 and BLF10M6LS135 are capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions:  $V_{DS}$  = 28 V;  $I_{Dq}$  = 950 mA;  $P_L$  = 135 W; f = 894 MHz.



## 7.2 Test circuit information



The striplines are on a double copper-clad Taconic RF35 Printed-Circuit Board (PCB) with  $\varepsilon_r$  = 3.5 and thickness = 0.76 mm. See <u>Table 9</u> for list of components.

## The drawing is not to scale.

#### Fig 2. Component layout

# Table 9.List of componentsSee Figure 1 and Figure 2.

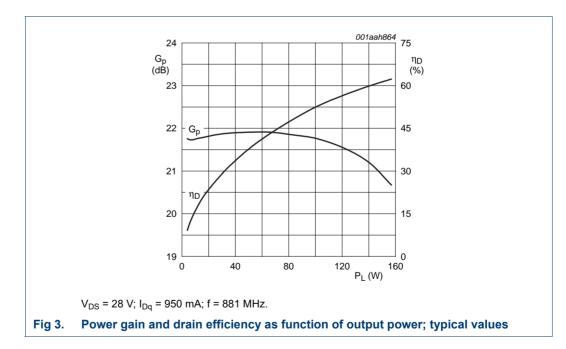
See <u>Figure 1</u> and <u>Figure 2</u> .				
Component	Description	Value	Remarks	
C1, C3, C10, C14, C17	multilayer ceramic chip capacitor	68 pF [	solder vertically	
C2, C4, C5	multilayer ceramic chip capacitor	8.2 pF	solder vertically	
C6, C7	multilayer ceramic chip capacitor	10 pF	solder vertically	
C8, C9, C12, C13	electrolytic capacitor	100 nF	Vishay or capacitor of same quality	
C11, C15	multilayer ceramic chip capacitor	4.7 μF, 50 V	2]	
C16	multilayer ceramic chip capacitor	3.0 pF [	solder vertically	
C18, C19, C20	electrolytic capacitor	220 μF, 63 V		
L1	ferrite SMD bead		Ferroxcube BDS 3/3/4.6-4S2 or equivalent	
Q1	BLF10M6135			
R1, R2, R3	SMD resistor	9.1 Ω, 0.1 W		

[1] American Technical Ceramics type 100B or capacitor of same quality.

[2] TDK or capacitor of same quality.

## 7.3 Graphical data

### 7.3.1 1-Tone CW



-20

-30

-40

-50

IMD

(dBc)

**Power LDMOS transistor** 

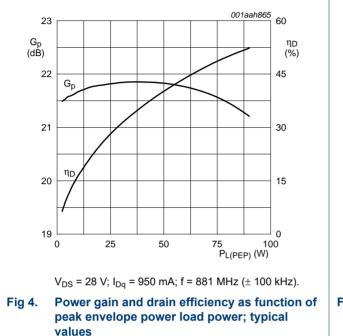
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IMD3

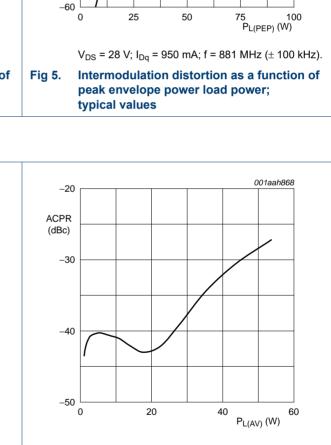
IMD5

IMD7

7.3.2 2-Tone CW

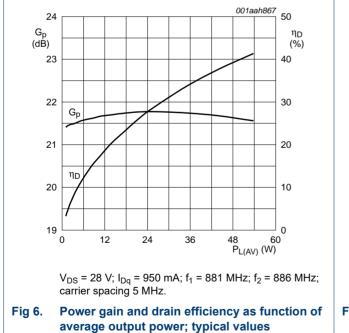


### 7.3.3 2-Carrier W-CDMA



 $V_{DS}$  = 28 V;  $I_{Dq}$  = 950 mA;  $f_1$  = 881 MHz;  $f_2$  = 886 MHz; carrier spacing 5 MHz.

Fig 7. Adjacent power channel ratio as a function of average output power; typical values

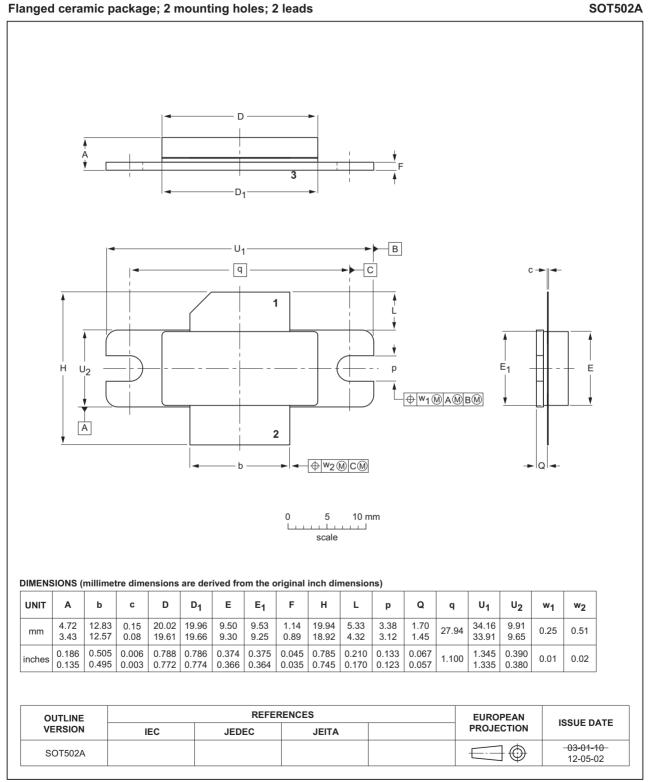


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# BLF10M6135; BLF10M6LS135

**Power LDMOS transistor** 

# 8. Package outline



### Fig 8. Package outline SOT502A

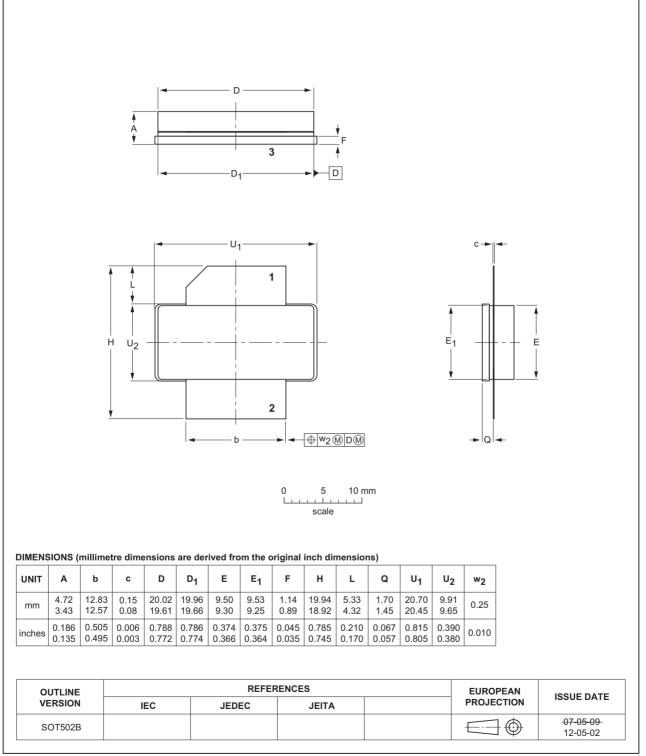
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### **Power LDMOS transistor**

SOT502B





### Fig 9. Package outline SOT502B

# 9. Handling information

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#### CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the ANSI/ESD S20.20, IEC/ST 61340-5, JESD625-A or equivalent standards.

# **10. Abbreviations**

Table 10. Abbre	Table 10. Abbreviations			
Acronym	Description			
3GPP	3rd Generation Partnership Project			
CCDF	Complementary Cumulative Distribution Function			
CW	Continuous Wave			
DPCH	Dedicated Physical CHannel			
ESD	ElectroStatic Discharge			
ISM	Industrial, Scientific and Medical			
LDMOS	Laterally Diffused Metal-Oxide Semiconductor			
PAR	Peak-to-Average Ratio			
SMD	Surface Mounted Device			
VSWR	Voltage Standing-Wave Ratio			
W-CDMA	Wideband Code Division Multiple Access			

## 11. Revision history

#### Table 11.Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLF10M6135_BLF10M6LS135#2	20150901	Product data sheet	-	BLF10M6135_BLF10 M6LS135 v.1
Modifications:	• The format of this document has been redesigned to comply with the new identity guidelines of Ampleon.			
	<ul> <li>Legal texts have been adapted to the new company name where appropriate</li> </ul>			me where appropriate.
BLF10M6135_BLF10M6LS135 v.1	20140624	Product data sheet	-	-

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Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
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