BLA8G1011L(S)-300; BLA8G1011L(S)-300G

Power LDMOS transistor

AMPLEON

Rev. 4 — 4 August 2016

Product data sheet

1. Product profile

1.1 General description

300 W LDMOS power transistor for avionics applications at frequencies from 1030 MHz to 1090 MHz.

Table 1. Test information

Typical RF performance at T_{case} = 25 °C in a class-AB production test circuit.

Test signal	f	V _{DS}	PL	G _p	η_D	t _r	t _f
	(MHz)	(V)	(W)	(dB)	(%)	(ns)	(ns)
pulsed RF	1060	32	300	16.5	56	14	5

1.2 Features and benefits

- Easy power control
- Integrated ESD protection
- Enhanced ruggedness
- High efficiency
- Excellent thermal stability
- Designed for broadband operation (1030 MHz to 1090 MHz)
- Internally matched for ease of use
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

1.3 Applications

Avionics transmitter applications in the 1030 MHz to 1090 MHz frequency range

2. Pinning information

Table 2. Pinning

Pin	Passwintian	Cimplified autiline	Cranbia aymbal
	Description	Simplified outline	Graphic symbol
	-300 (SOT502A)		
1	drain		4
2	gate	1 S 3	<u> </u>
3	source [1]		2 —
			3
			sym112
BLA8G1011L	S-300 (SOT502B)		
1	drain		
2	gate	1 3	ئے.
3	source [1]		2 1
			3
			sym112
BLA8G1011L	-300G (SOT502F)		
1	drain		
2	gate	1	1 L
3	source [1]	$\frac{1}{2}$	2 1
		2	3
			sym112
BLA8G1011L	S-300G (SOT502E)		
1	drain		
2	gate		1
3	source [1]		2 4
		2 3	3
			sym112
	1	1	1

^[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Packag	e	
	Name	Description	Version
BLA8G1011L-300	-	flanged ceramic package; 2 mounting holes; 2 leads	SOT502A
BLA8G1011LS-300	-	earless flanged ceramic package; 2 leads	SOT502B
BLA8G1011L-300G	-	eared flanged ceramic package; 2 leads; 2 mounting holes	SOT502F
BLA8G1011LS-300G	-	earless flanged ceramic package; 2 leads	SOT502E

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	65	V
V_{GS}	gate-source voltage		-0.5	+13	V
T _{stg}	storage temperature		-65	+150	°C
Tj	junction temperature	[1]	-	225	°C

^[1] Continuous use at maximum temperature will affect the reliability, for details refer to the on-line MTF calculator.

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Тур	Unit
$Z_{th(j-c)}$	transient thermal impedance from junction to	$T_{case} = 25 ^{\circ}C; t_p = 10 \mu s;$	0.112	K/W
,	case	δ = 10 %		

6. Characteristics

Table 6. DC characteristics

 T_i = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V _{(BR)DSS}	drain-source breakdown voltage	$V_{GS} = 0 \text{ V}; I_D = 4.5 \text{ mA}$	65	-	-	V
V _{GS(th)}	gate-source threshold voltage	V _{DS} = 10 V; I _D = 450 mA	1.5	1.8	2.3	V
I _{DSS}	drain leakage current	V _{GS} = 0 V; V _{DS} = 28 V	-	-	4.2	μА
I _{DSX}	drain cut-off current	$V_{GS} = V_{GS(th)} + 3.75 \text{ V};$ $V_{DS} = 10 \text{ V}$	67.9	82	-	A
I _{GSS}	gate leakage current	V _{GS} = 11 V; V _{DS} = 0 V	-	-	420	nA
9 _{fs}	forward transconductance	V_{DS} = 10 V; I_{D} = 450 mA	2.67	3.92	5.25	S
R _{DS(on)}	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75 V;$ $I_D = 15.75 A$	0.008	0.04	0.079	Ω

Table 7. RF characteristics

Test signal: pulsed RF; t_p = 50 μ s; δ = 2 %; V_{DS} = 32 V; f = 1060 MHz; I_{Dq} = 150 mA; T_{case} = 25 °C; unless otherwise specified; in a class-AB production test circuit for straight leads.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Gp	power gain	P _L = 300 W	15	16.5	-	dB
RLin	input return loss	P _L = 300 W	-	-16	-11	dB
η_{D}	drain efficiency	P _L = 300 W	52	56	-	%
t _r	rise time	P _L = 300 W	-	14	-	ns
t _f	fall time	P _L = 300 W	-	5	-	ns

7. Test information

7.1 Ruggedness in class-AB operation

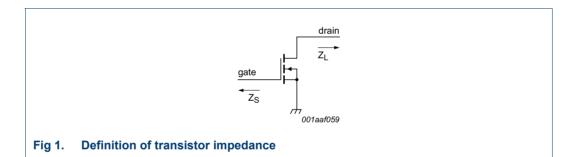
The BLA8G1011L-300, BLA8G1011LS-300, BLA8G1011L-300G and BLA8G1011LS-300G are enhanced rugged devices and are capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: t_p = 50 μ s; δ = 2 %; V_{DS} = 32 V; I_{Dq} = 100 mA; P_L = 300 W; f = 1030 MHz to 1090 MHz.

7.2 Impedance information

Table 8. Typical impedance

Typical values unless otherwise specified.

f	Z _S	Z _L
(MHz)	(Ω)	(Ω)
1000	2.84 – j3.69	0.80 - j1.00
1050	3.98 – j3.26	0.62 – j1.26
1100	5.22 – j2.92	0.66 – j1.17



7.3 Test circuit

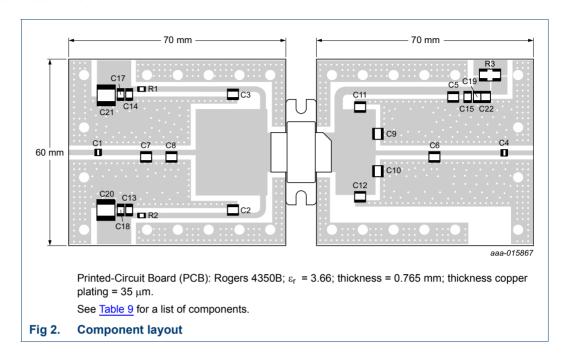
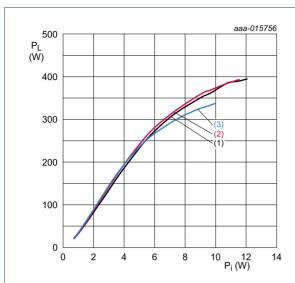


Table 9. List of componentsSee Figure 2 for component layout.

Component	Description	Value	Remarks
C1, C4	multilayer ceramic chip capacitor	91 pF	ATC: ATC100A910FT150XT
C2, C3, C5	multilayer ceramic chip capacitor	39 pF	ATC: ATC100B390FT500XTV
C6	multilayer ceramic chip capacitor	1.5 pF	ATC: ATC800B1R5BT500XTV
C7	multilayer ceramic chip capacitor	3.3 pF	ATC: ATC100B3R3BT500XTV
C8	multilayer ceramic chip capacitor	2.4 pF	ATC: ATC100B2R4BT500XTV
C9, C10	multilayer ceramic chip capacitor	0.6 pF	ATC: ATC100B0R6BT500XTV
C11, C12	multilayer ceramic chip capacitor	2.7 pF	ATC: ATC100B2R7BT500XTV
C13, C14, C15	multilayer ceramic chip capacitor	0.1 μF	Murata: GRM31C5C1H104JA01K
C17, C18, C19	multilayer ceramic chip capacitor	1 μF	Murata: GRM31MR71H105KA88L
C20, C21	multilayer ceramic chip capacitor	4.7 μF	TDK: C5750X7R2A475K230KA
C22	multilayer ceramic chip capacitor	4.7 μF	Murata: GRM32ER71H475KA88L
R1, R2	SMD resistor	9.1 Ω	Yageo: RC0805FR-079R1L
R3	SMD resistor	0.01 Ω	Ohmite: LVK25R010FER

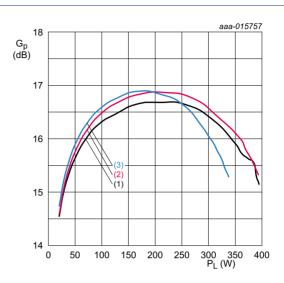
7.4 Graphical data



 V_{DS} = 32 V; I_{Dq} = 150 mA; t_p = 50 μs ; δ = 2 %.

- (1) f = 1030 MHz
- (2) f = 1060 MHz
- (3) f = 1090 MHz

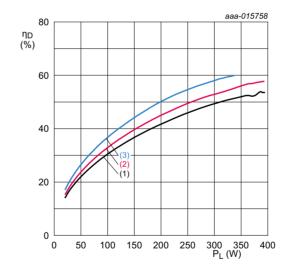
Fig 3. Output power as a function of input power; typical values



 V_{DS} = 32 V; I_{Dq} = 150 mA; t_p = 50 μ s; δ = 2 %.

- (1) f = 1030 MHz
- (2) f = 1060 MHz
- (3) f = 1090 MHz

Fig 4. Power gain as a function of output power; typical values



 V_{DS} = 32 V; I_{Dq} = 150 mA; t_p = 50 μ s; δ = 2 %.

- (1) f = 1030 MHz
- (2) f = 1060 MHz
- (3) f = 1090 MHz

Fig 5. Drain efficiency as a function of output power; typical values

Package outline

Flanged ceramic package; 2 mounting holes; 2 leads

SOT502A

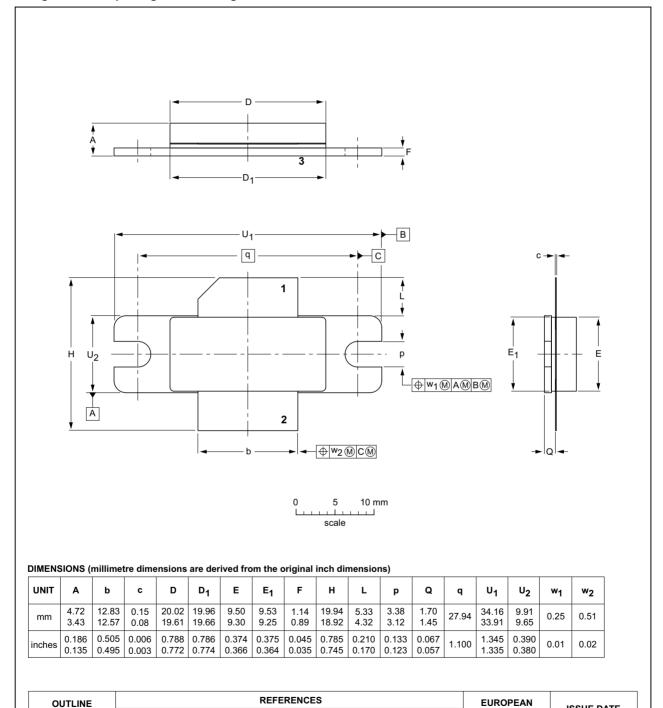


Fig 6. Package outline SOT502A

IEC

JEDEC

VERSION

SOT502A

JEITA

ISSUE DATE

03-01-10

12-05-02

PROJECTION

Earless flanged ceramic package; 2 leads

SOT502B

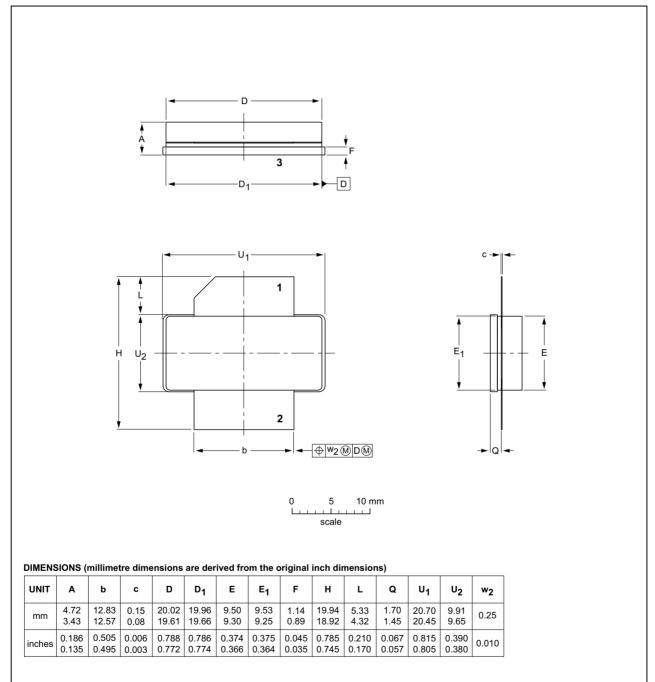


Fig 7. Package outline SOT502B

IEC

OUTLINE

VERSION

SOT502B

JEITA

REFERENCES

JEDEC

ISSUE DATE

07-05-09

12-05-02

EUROPEAN

PROJECTION

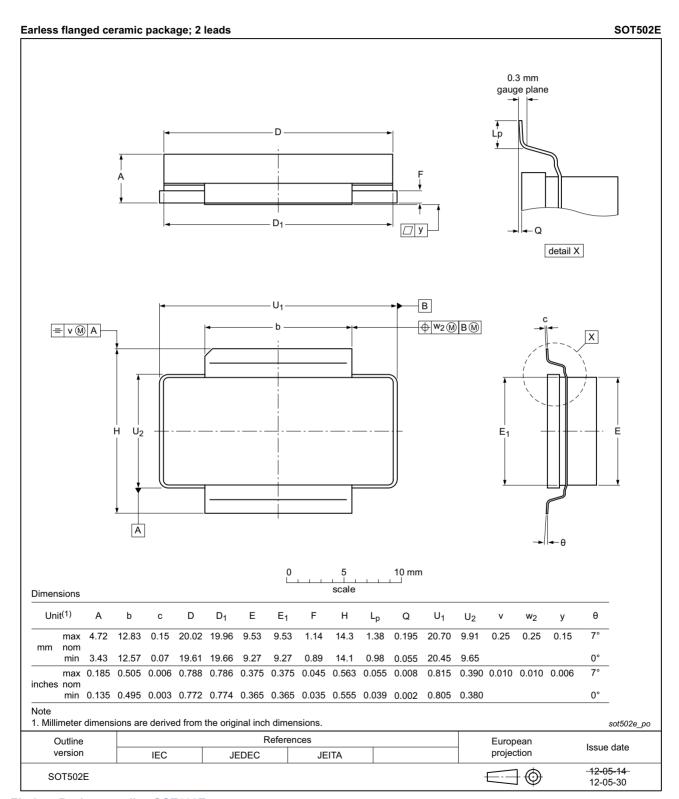


Fig 8. Package outline SOT502E

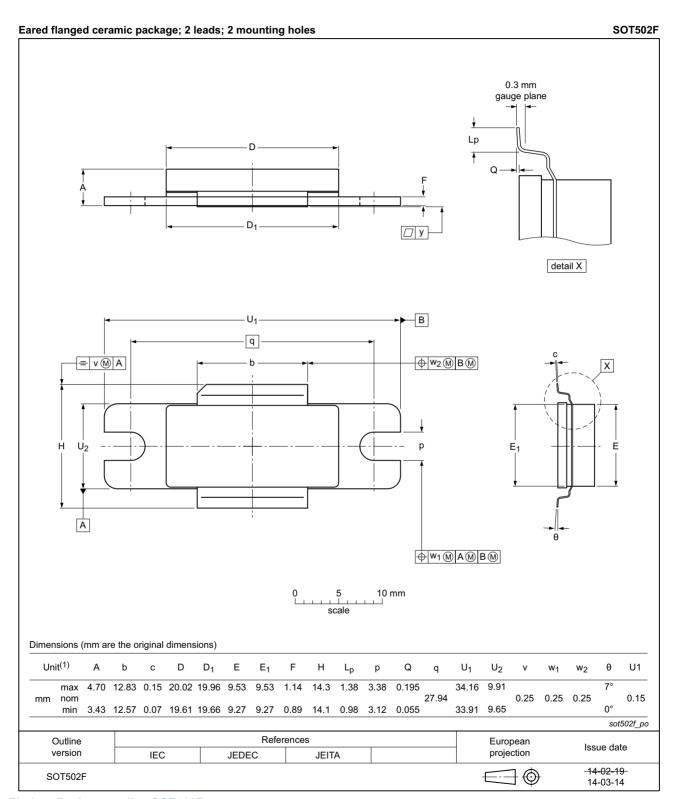


Fig 9. Package outline SOT502F

9. Handling information

CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the ANSI/ESD S20.20, IEC/ST 61340-5, JESD625-A or equivalent standards.

10. Abbreviations

Table 10. Abbreviations

Acronym	Description
ESD	ElectroStatic Discharge
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
MTF	Median Time to Failure
SMD	Surface Mounted Device
VSWR	Voltage Standing-Wave Ratio

11. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLA8G1011L-300_LS-300_L-300G _LS-300G v.4	20160804	Product data sheet		BLA8G1011L-300_LS-300 _L-300G_LS-300G v.3
Modifications:	• Table 9 on	page 5: row 4 to row 7, v	alue units correct	ted from nF to pF
BLA8G1011L-300_LS-300_L-300G _LS-300G v.3	20150901	Product data sheet		BLA8G1011L-300_LS-300 _L-300G_LS-300G v.2
BLA8G1011L-300_LS-300_L-300G _LS-300G v.2	20150126	Product data sheet		BLA8G1011L-300_LS-300 _L-300G_LS-300G v.1
BLA8G1011L-300_LS-300_L-300G _LS-300G v.1	20140929	Objective data sheet		-

12. Legal information

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Document status[1][2]	Product status[3]	Definition	
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.	
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.	
Product [short] data sheet	Production	This document contains the product specification.	

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BLA8G1011L(S)-300(G)

Power LDMOS transistor

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Power LDMOS transistor

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