# BLA1011-200R; BLA1011S-200R

# **Avionics LDMOS transistors**

**AMPLEON** 

Rev. 2 — 1 September 2015

Product data sheet

### 1. Product profile

#### 1.1 General description

200 W LDMOS avionics power transistor for transmitter applications at frequencies from 1030 MHz to 1090 MHz.

#### Table 1. Typical performance

RF performance at  $T_h$  = 25 °C in a common source class-AB test circuit;  $I_{Dq}$  = 150 mA; typical values.

Mode of operation	Conditions	V <sub>DS</sub> (V)	P <sub>L</sub> (W)	G <sub>p</sub> (dB)	η <sub>D</sub> (%)	t <sub>r</sub> (ns)	t <sub>f</sub> (ns)
Pulsed class-AB:	$t_p$ = 50 $\mu$ s; $\delta$ = 2 %	36	200	15	50	35	6
1030 MHz to 1090 MHz	$t_p$ = 128 $\mu$ s; $\delta$ = 2 %	36	250	14	50	35	6
	$t_p$ = 340 $\mu$ s; $\delta$ = 1 %	36	250	14	50	35	6

#### CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Therefore care should be taken during transport and handling.

#### 1.2 Features and benefits

- Typical pulsed class-AB performance at a frequencies from 1030 MHz to 1090 MHz, a supply voltage of 36 V and an I<sub>Dq</sub> of 150 mA:
  - ◆ Load power ≥ 200 W
  - ◆ Gain ≥ 13 dB
  - ◆ Efficiency ≥ 45 %
  - ◆ Rise time ≤ 50 ns
  - ◆ Fall time ≤ 50 ns
- High power gain
- Easy power control
- Excellent ruggedness
- Source on mounting flange eliminates DC isolators, reducing common mode inductance
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

### 1.3 Applications

Avionics transmitter applications in the 1030 MHz to 1090 MHz frequency range.

### 2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
BLA1011-	200R (SOT502A)		
1	drain		
2	gate		1 
3	source		2—
			3 sym039
BLA10118	S-200R (SOT502B)		
1	drain		
2	gate	1 3	1 
3	source	[1]	2
			3 sym039

<sup>[1]</sup> Connected to flange.

### 3. Ordering information

Table 3. Ordering information

Type number	Packag	ıckage					
	Name	Description	Version				
BLA1011-200R	-	flanged LDMOST ceramic package; 2 mounting holes; 2 leads	SOT502A				
BLA1011S-200R	-	earless flanged LDMOST ceramic package; 2 leads	SOT502B				

### 4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage		-	75	V
$V_{GS}$	gate-source voltage		-	±22	V
P <sub>tot</sub>	total power dissipation	$T_h \leq 25~^{\circ}\text{C};~t_p$ = 50 $\mu\text{s};~\delta$ = 2 %	-	700	W
T <sub>stg</sub>	storage temperature		-65	+150	°C
Tj	junction temperature		-	200	°C

#### 5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Тур	Unit
$Z_{\text{th(j-h)}}$	transient thermal impedance from junction to heatsink	T <sub>h</sub> = 25 °C	<u>11</u> 0.15	K/W

<sup>[1]</sup> Thermal resistance is determined under RF operating conditions;  $t_p = 50 \mu s$ ,  $\delta = 10 \%$ .

#### 6. Characteristics

Table 6. Characteristics

 $T_i = 25$  °C unless otherwise specified

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS}$ = 0 V; $I_D$ = 3 mA	75	-	-	V
V <sub>GS(th)</sub>	gate-source threshold voltage	$V_{DS}$ = 10 V; $I_{D}$ = 300 mA	4	-	5	V
I <sub>DSS</sub>	drain leakage current	$V_{GS} = 0 \text{ V}; V_{DS} = 36 \text{ V}$	-	-	1	μА
I <sub>DSX</sub>	drain cut-off current	$V_{GS} = V_{GS(th)} + 9 V;$ $V_{DS} = 10 V$	45	-	-	Α
I <sub>GSS</sub>	gate leakage current	$V_{GS} = \pm 20 \text{ V}; V_{DS} = 0 \text{ V}$	-	-	1	μА
9 <sub>fs</sub>	forward transconductance	$V_{DS} = 10 \text{ V}; I_D = 10 \text{ A}$	-	9	-	S
R <sub>DS(on)</sub>	drain-source on-state resistance	$V_{GS} = 9 \text{ V}; I_D = 10 \text{ A}$	-	60	-	$m\Omega$

### 7. Application information

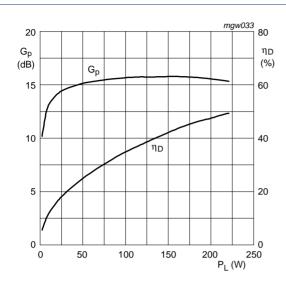
#### Table 7. Application information

RF performance in a common source pulsed class-AB circuit; ( $t_p$  = 50  $\mu$ s;  $\delta$  = 2 %); f = 1030 MHz and 1090 MHz;  $T_h$  = 25 °C;  $Z_{th(mb-h)}$  = 0.15 K/W;  $I_{Dq}$  = 150 mA; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
$V_{DS}$	drain-source voltage		-	36	-	V
$P_{L}$	output power	$t_p$ = 50 $\mu$ s; $\delta$ = 2 %	-	200		W
Gp	power gain	P <sub>L</sub> = 200 W	13	-		dB
$\eta_{D}$	drain efficiency	$t_p$ = 50 $\mu$ s; $\delta$ = 2 %	45	-		%
t <sub>r</sub>	rise time		-	-	50	ns
t <sub>f</sub>	fall time		-	-	50	ns

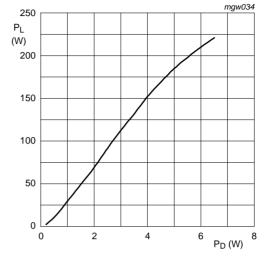
#### 7.1 Ruggedness in class-AB operation

The BLA1011-200R and BLA1011S-200R are capable of withstanding a load mismatch corresponding to VSWR = 5:1 through all phases under the following conditions:  $V_{DS} = 36 \text{ V}$ ; f = 1030 MHz to 1090 MHz at rated load power.



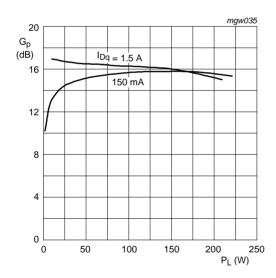
 $V_{DS}$  = 36 V;  $I_{Dq}$  = 150 mA; f = 1060 MHz;  $t_p$  = 50  $\mu s;$   $\delta$  = 2 %

Fig 1. Power gain and drain efficiency as functions of load power; typical values



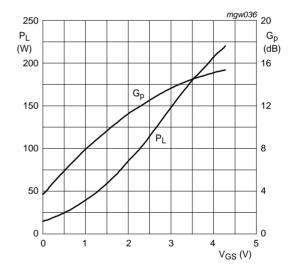
 $V_{DS}$  = 36 V;  $I_{Dq}$  = 150 mA; f = 1060 MHz;  $t_p$  = 50  $\mu s;$   $\delta$  = 2 %

Fig 2. Load power as a function of drive power; typical values



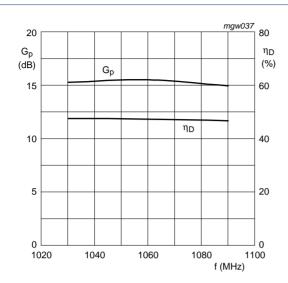
 $V_{DS}$  = 36 V; f = 1060 MHz;  $t_p$  = 50  $\mu$ s;  $\delta$  = 2 %

Fig 3. Power gain as a function of load power; typical values



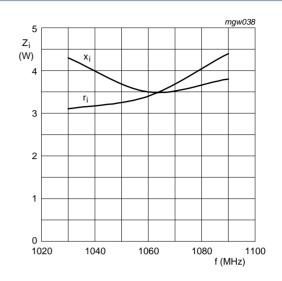
 $V_{DS}$  = 36 V;  $I_{Dq}$  = 150 mA;  $P_{i}$  = 5.5 W; f = 1060 MHz;  $t_{p}$  = 50  $\mu$ s;  $\delta$  = 2 %

Fig 4. Load power and power gain as functions of gate-source voltage; typical values



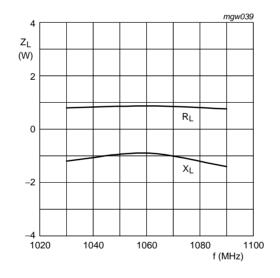
 $V_{DS}$  = 36 V;  $I_{Dq}$  = 150 mA;  $P_L$  = 200 W;  $t_p$  = 50  $\mu s;$   $\delta$  = 2 %

Fig 5. Power gain and drain efficiency a functions of frequency; typical values



 $V_{DS}$  = 36 V;  $I_{Dq}$  = 150 mA;  $P_L$  = 200 W;  $t_p$  = 50  $\mu s;$   $\delta$  = 2 %

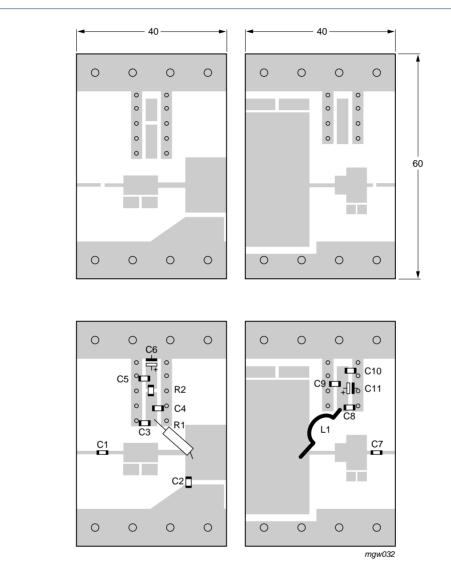
Fig 6. Input Impedance as a function of frequency (series components); typical values



 $V_{DS}$  = 36 V;  $I_{Dq}$  = 150 mA;  $P_L$  = 200 W;  $t_p$  = 50  $\mu s;$   $\delta$  = 2 %

Fig 7. Load impedance as a function of frequency (series components); typical values

### 8. Test information



Dimensions in mm.

The components are situated on one side of the copper-clad Duroid Printed-Circuit Board (PCB) with  $\epsilon_r$  = 6.2 and thickness 0.64 mm.

The other side is unetched and serves as a ground plane.

See Table 8 for list of components.

Fig 8. Component layout for 1030 MHz to 1090 MHz test circuit

Table 8. List of components (see Figure 8)

Component	Description		Value	Dimensions
C1	multilayer ceramic chip capacitor	[1]	39 pF	
C2	multilayer ceramic chip capacitor	[2]	4.3 pF	
C3	multilayer ceramic chip capacitor	<u>[1]</u>	11 pF	
C4, C7	multilayer ceramic chip capacitor	<u>[1]</u>	62 pF	
C5	multilayer ceramic chip capacitor	<u>[1]</u>	100 pF	
C6	electrolytic capacitor		$47~\mu F;20~V$	
C8	multilayer ceramic chip capacitor	[2]	20 pF	
C9	multilayer ceramic chip capacitor	<u>[1]</u>	47 pF	
C10	multilayer ceramic chip capacitor	[3]	1.2 nF	
C11	electrolytic capacitor		$47~\mu F;63~V$	
L1	$\Omega\text{-shaped enamelled 1 mm copper wire}$			length = 38 mm
R1	metal film resistor		301 Ω	
R2	SMD 0508 resistor		18 Ω	

<sup>[1]</sup> American Technical Ceramics type 100A or capacitor of same quality.

<sup>[2]</sup> American Technical Ceramics type 100B or capacitor of same quality.

<sup>[3]</sup> American Technical Ceramics type 700 or capacitor of same quality.

### 9. Package outline

Flanged ceramic package; 2 mounting holes; 2 leads

SOT502A

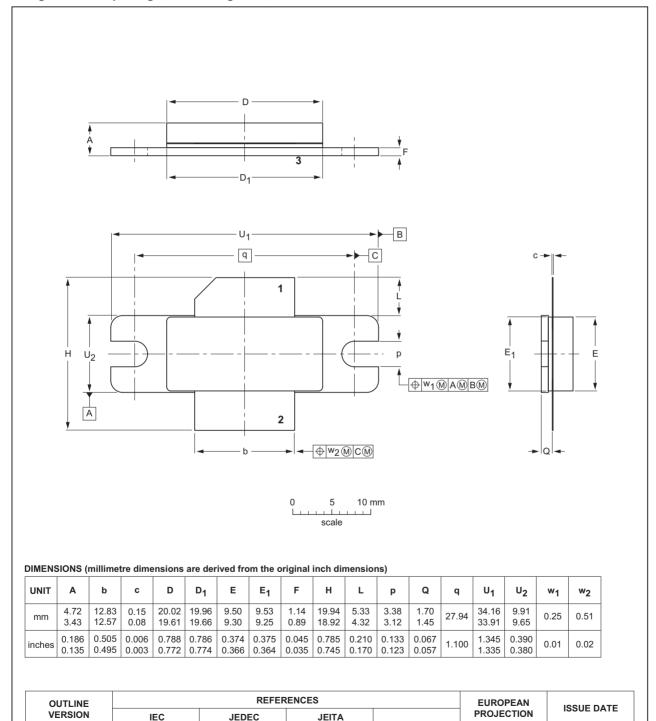


Fig 9. Package outline SOT502A

SOT502A

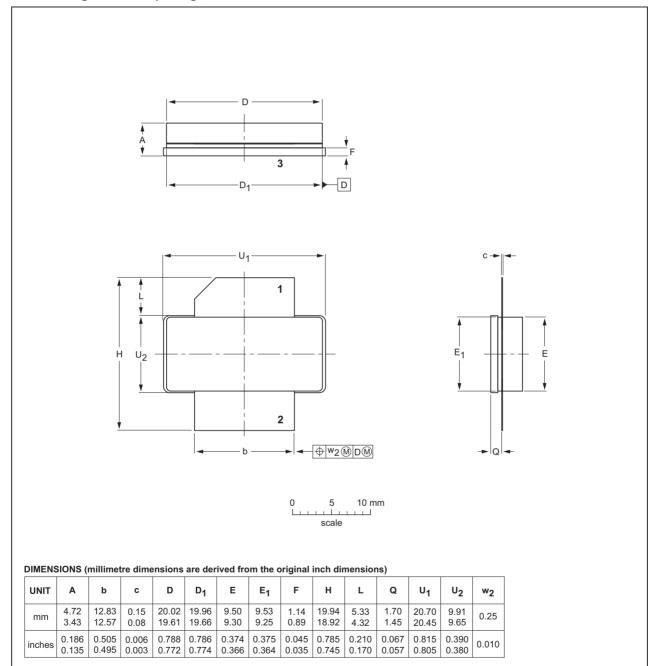
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03-01-10

12-05-02

#### Earless flanged ceramic package; 2 leads

SOT502B



#### Fig 10. Package outline SOT502B

IEC

OUTLINE

**VERSION** 

SOT502B

**JEITA** 

REFERENCES

**JEDEC** 

**ISSUE DATE** 

07-05-09

12-05-02

**EUROPEAN** 

**PROJECTION** 

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### 10. Abbreviations

Table 9. Abbreviations

Acronym	Description
$I_{Dq}$	quiescent drain current
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
LDMOST	Laterally Diffused Metal-Oxide Semiconductor Transistor
RF	Radio Frequency
SMD	Surface Mount Device
VSWR	Voltage Standing-Wave Ratio

### 11. Revision history

#### Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes		
BLA1011-200R_1011S-200R#2	20150901	Product data sheet	-	BLA1011-200R_1011S-200R_1		
Modifications:		The format of this document has been redesigned to comply with the new identity guidelines of Ampleon.				
	Legal texts have been adapted to the new company name where appropriate.					
BLA1011-200R_1011S-200R_1	20100223	Product data sheet	-	-		

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Document status[1][2]	Product status[3]	Definition
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#### **Avionics LDMOS transistors**

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