ART2K0PE; ART2K0PEG

Power LDMOS transistor

AMPLEON

Rev. 5 — 7 August 2024

Product data sheet

1. Product profile

1.1 General description

Based on Advanced Rugged Technology (ART), this 2000 W LDMOS RF power transistor has been designed to cover a wide range of applications for ISM, broadcast and communications. The unmatched transistor has a frequency range of 1 MHz to 450 MHz.

Table 1. Application information

Test signal	f	V_{DS}	P_L	G_p	η_D
	(MHz)	(V)	(W)	(dB)	(%)
CW	41	65	1600	28.8	79.4
CW pulsed [1][2]	60	55	1250	24.7	85.8
CW pulsed [1][2]	60	65	1690	25.1	83.3
CW pulsed [1][2]	64	65	1785	25.7	84.7
CW [3]	87.5 to 108	60	1730	25.8	85.1

[1] t_p = 100 μs; δ = 10 %.

[2] Performance at 3 dB gain compression level.

[3] Center band performance numbers across the indicated frequency range.

1.2 Features and benefits

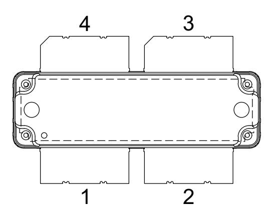
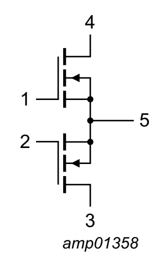
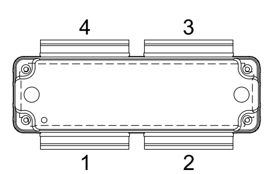
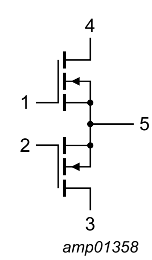
- High breakdown voltage enables class E operation up to V_{DS} = 53 V
- Qualified up to a maximum of V_{DS} = 65 V
- Characterized from 30 V to 65 V to support a wide range of applications
- Integrated dual sided ESD protection enables class C operation and complete switch off of the transistor
- Excellent ruggedness with no device degradation
- High efficiency
- Excellent thermal stability
- Designed for broadband operation
- For RoHS compliance see the product details on the Ampleon website

1.3 Applications

- Industrial, scientific and medical applications
    - Plasma generators
    - MRI systems
    - Particle accelerators
- Broadcast
    - FM radio
    - VHF TV
- Communications
    - Non cellular communications
    - UHF radar

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
ART2K0PE (OMP-1230-4F-1)			
1	gate1		
2	gate2		
3	drain2		
4	drain1		
5	source [1]		
ART2K0PEG (OMP-1230-4G-1)			
1	gate1		
2	gate2		
3	drain2		
4	drain1		
5	source [1]		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Package name	Orderable part number	12NC	Packing description	Min. orderable quantity (pieces)
OMP-1230-4F-1	ART2K0PEZ	9349 606 96517	Tray; 20-fold; dry pack	60
	ART2K0PEY	9349 606 96518	TR13; 100-fold; 56 mm; dry pack	100
OMP-1230-4G-1	ART2K0PEGZ	9349 606 97517	Tray; 20-fold; dry pack	60
	ART2K0PEGY	9349 606 97518	TR13; 100-fold; 56 mm; dry pack	100

4. Limiting values

Table 4. Limiting values
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	[1]	-	200	V
V_{GS}	gate-source voltage		–9	+13	V
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature	[2]	-	225	°C

[1] Specified over lifetime at maximum operating temperature.

[2] Continuous use at maximum temperature will affect the reliability.

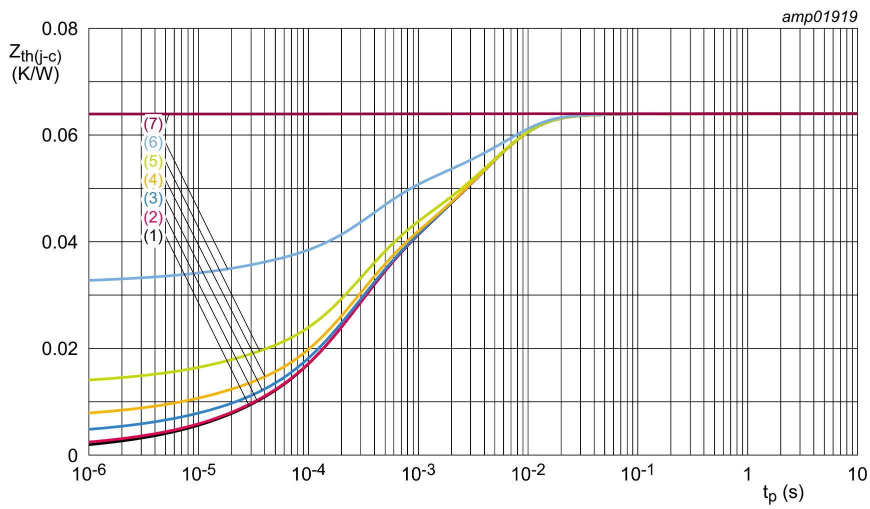
5. Thermal characteristics

Table 5. Thermal characteristics
According to standard MIL-STD-883E.

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	T_j = 95 °C, measured under RF condition [1][2]	0.064	K/W

[1] Refer to application note *AN221014* on the Ampleon website.

[2] See Figure 1.



(1) δ = 0.1 % (single push)
(2) δ = 1 %
(3) δ = 5 %
(4) δ = 10 %
(5) δ = 20 %
(6) δ = 50 %
(7) δ = 100 % (steady state)

Fig 1. Transient thermal impedance from junction to case as a function of pulse duration

6. Characteristics

Table 6. DC characteristics

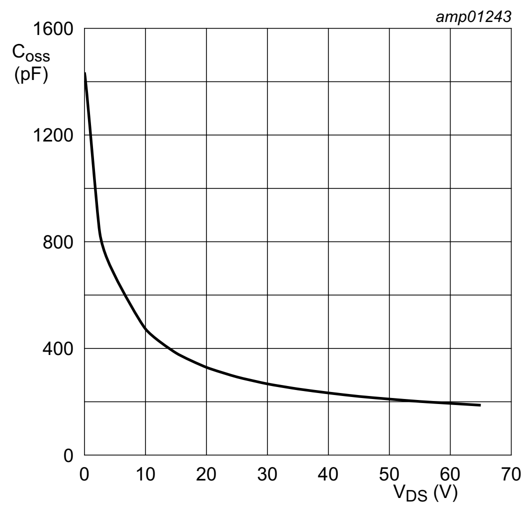
T_j = 25 °C; per section unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 5.5 mA	203	208	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 20 V; I_D = 550 mA	1.6	2.1	2.6	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 65 V	-	-	2.8	μA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 3.75 V; V_{DS} = 20 V	-	76	-	A
I_{GSS}	gate leakage current	V_{GS} = 11 V; V_{DS} = 0 V	-	-	280	nA
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 3.75 V; I_D = 19.25 A	-	0.106	-	Ω

Table 7. AC characteristics

T_j = 25 °C; per section unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{rs}	feedback capacitance	V_{GS} = 0 V; V_{DS} = 65 V; f = 1 MHz	-	3.27	-	pF
C_{iss}	input capacitance	V_{GS} = 0 V; V_{DS} = 65 V; f = 1 MHz	-	614	-	pF
C_{oss}	output capacitance	V_{GS} = 0 V; V_{DS} = 65 V; f = 1 MHz	-	187	-	pF



V_{GS} = 0 V; f = 1 MHz

Fig 2. Output capacitance as a function of drain-source voltage; typical values per section

Table 8. RF characteristics

Test signal: pulsed RF; t_p = 100 μs; δ = 3 %; f = 108 MHz; RF performance at V_{DS} = 65 V; I_{Dq} = 50 mA per section; T_{case} = 25 °C; unless otherwise specified; in a class-AB production test circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	P_L = 2000 W	26.5	27.7	-	dB
RL_{in}	input return loss	P_L = 2000 W	-	−15	-	dB
η_D	drain efficiency	P_L = 2000 W	68.0	71.7	-	%

7. Test information

7.1 Ruggedness in class-AB operation

The ART2K0PE and ART2K0PEG are capable of withstanding a load mismatch corresponding to VSWR ≥ 65 : 1 through all phases under the following conditions: V_{DS} = 65 V; I_{Dq} = 100 mA per section; P_L = 2000 W pulsed; t_p = 100 μs; δ = 10 %; f = 108 MHz.

7.2 Impedance information

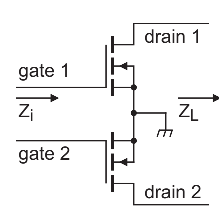
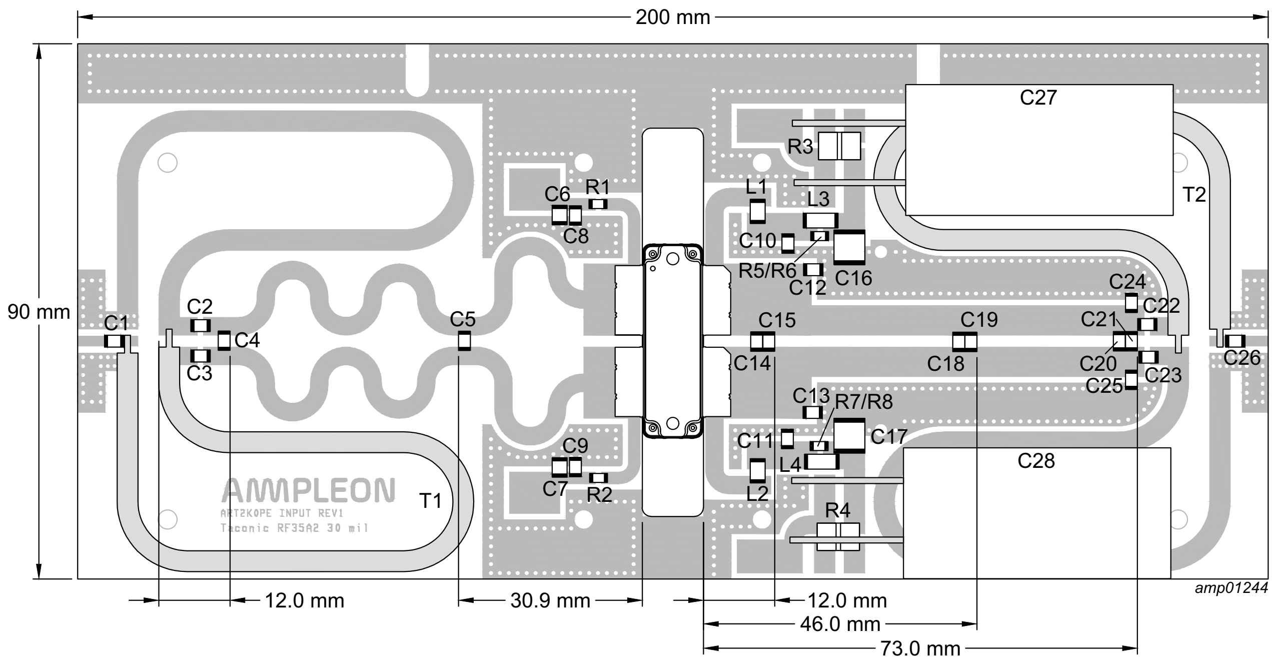


Fig 3. Definition of transistor impedance

Table 9. Typical push-pull impedance
Simulated Z_i and Z_L device impedance; impedance info at V_{DS} = 65 V and P_L = 2000 W.

f	Z_i	Z_L
(MHz)	**(Ω)**	**(Ω)**
108	2.4 – j8.7	3.8 + j0.9

7.3 Test circuit



Printed-Circuit Board (PCB): RF-35; ε_r = 3.5 F/m; thickness = 0.762 mm.

See Table 10 for a list of components.

Fig 4. Component layout

Table 10. List of components
For test circuit see Figure 4.

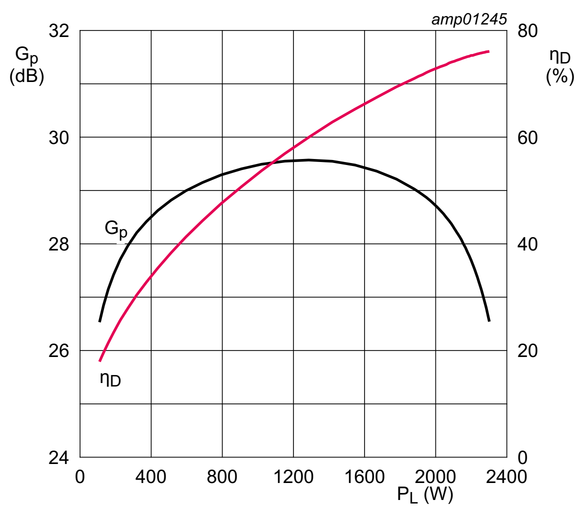
Component	Description	Value	Remarks
C1, C26	multilayer ceramic chip capacitor	470 pF [1]	
C2, C3	multilayer ceramic chip capacitor	68 pF [1]	
C4	multilayer ceramic chip capacitor	43 pF [1]	
C5	multilayer ceramic chip capacitor	300 pF [1]	
C6, C7	multilayer ceramic chip capacitor	4.7 μF, 50 V	Murata: GRM32ER71H475KA88L
C8, C9, C10, C11	multilayer ceramic chip capacitor	820 pF [1]	
C12, C13	multilayer ceramic chip capacitor	180 pF [1]	
C14, C15	multilayer ceramic chip capacitor	39 pF [1]	
C16, C17	multilayer ceramic chip capacitor	4.7 μF, 100 V	TDK: C5750X7R2A475KT/A
C18, C19	multilayer ceramic chip capacitor	56 pF [1]	
C20, C21	multilayer ceramic chip capacitor	51 pF [1]	

Table 10. List of components *…continued*
For test circuit see Figure 4.

Component	Description	Value	Remarks
C22, C23	multilayer ceramic chip capacitor	120 pF [1]	
C24, C25	multilayer ceramic chip capacitor	20 pF [1]	
C27, C28	electrolytic capacitor	2200 μF, 100 V	
L1, L2	air inductor	47 nH	Coilcraft: 1515SQ-47N
L3, L4	air inductor	82 nH	Coilcraft: 1515SQ-82N
R1, R2	resistor	4.7 kΩ	SMD 1206
R3, R4	resistor	0.01 Ω	Vishay: WSHP2818
R5, R6, R7, R8	resistor	9.1 Ω	SMD 1206
T1, T2	semi rigid coax	50 Ω, 160 mm	EZ141-AL-TP/M17

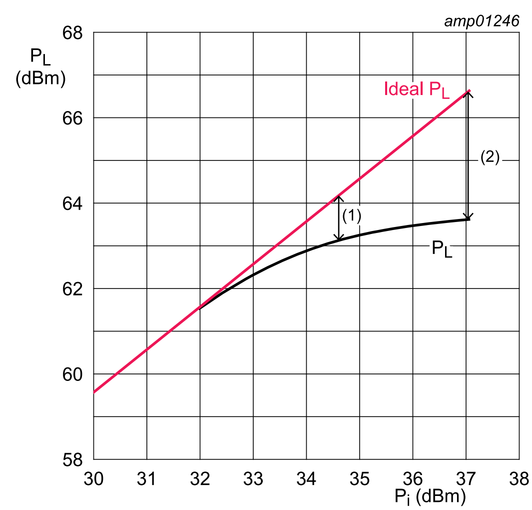
[1] American Technical Ceramics type 100B or capacitor of same quality.

7.4 Graphical data



V_{DS} = 65 V; I_{Dq} = 100 mA per section; f = 108 MHz; t_p = 100 μs; δ = 10 %.

Fig 5. Power gain and drain efficiency as function of output power; typical values

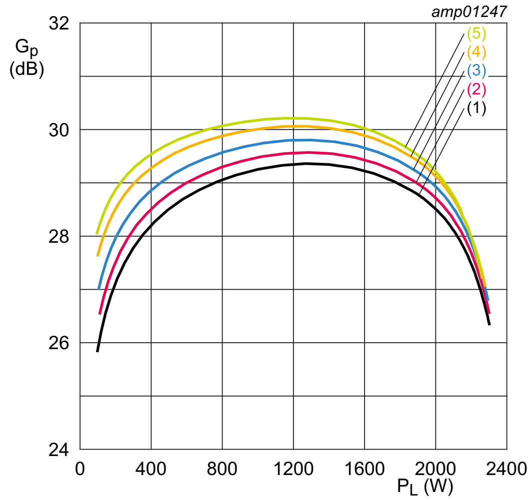


V_{DS} = 65 V; I_{Dq} = 100 mA per section; f = 108 MHz; t_p = 100 μs; δ = 10 %.

(1) $P_{L(1dB)}$ = 63.20 dBm (2045 W)

(2) $P_{L(3dB)}$ = 63.71 dBm (2300 W)

Fig 6. Output power as a function of input power; typical values



V_{DS} = 65 V; f = 108 MHz; t_p = 100 μs; δ = 10 %.

(1) I_{Dq} = 50 mA per section

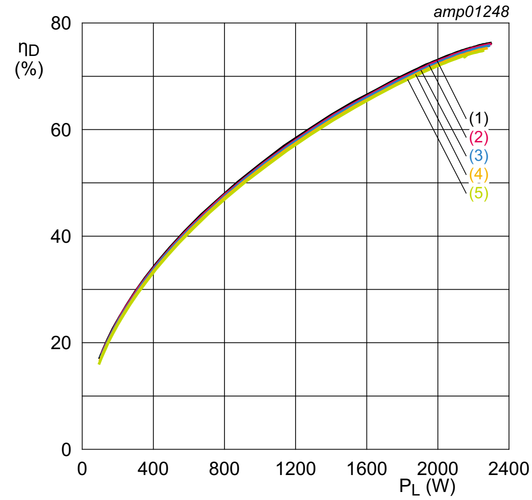
(2) I_{Dq} = 100 mA per section

(3) I_{Dq} = 200 mA per section

(4) I_{Dq} = 400 mA per section

(5) I_{Dq} = 600 mA per section

Fig 7. Power gain as a function of output power; typical values



V_{DS} = 65 V; f = 108 MHz; t_p = 100 μs; δ = 10 %.

(1) I_{Dq} = 50 mA per section

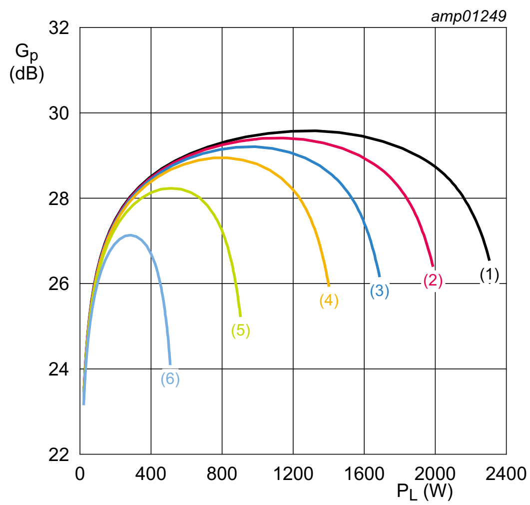
(2) I_{Dq} = 100 mA per section

(3) I_{Dq} = 200 mA per section

(4) I_{Dq} = 400 mA per section

(5) I_{Dq} = 600 mA per section

Fig 8. Drain efficiency as a function of output power; typical values



I_{Dq} = 100 mA per section; f = 108 MHz; t_p = 100 μs; δ = 10 %.

(1) V_{DS} = 65 V

(2) V_{DS} = 60 V

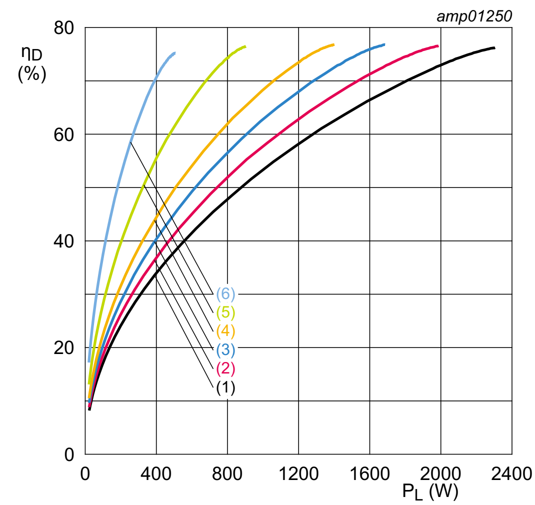
(3) V_{DS} = 55 V

(4) V_{DS} = 50 V

(5) V_{DS} = 40 V

(6) V_{DS} = 30 V

Fig 9. Power gain as a function of output power; typical values



I_{Dq} = 100 mA per section; f = 108 MHz; t_p = 100 μs; δ = 10 %.

(1) V_{DS} = 65 V

(2) V_{DS} = 60 V

(3) V_{DS} = 55 V

(4) V_{DS} = 50 V

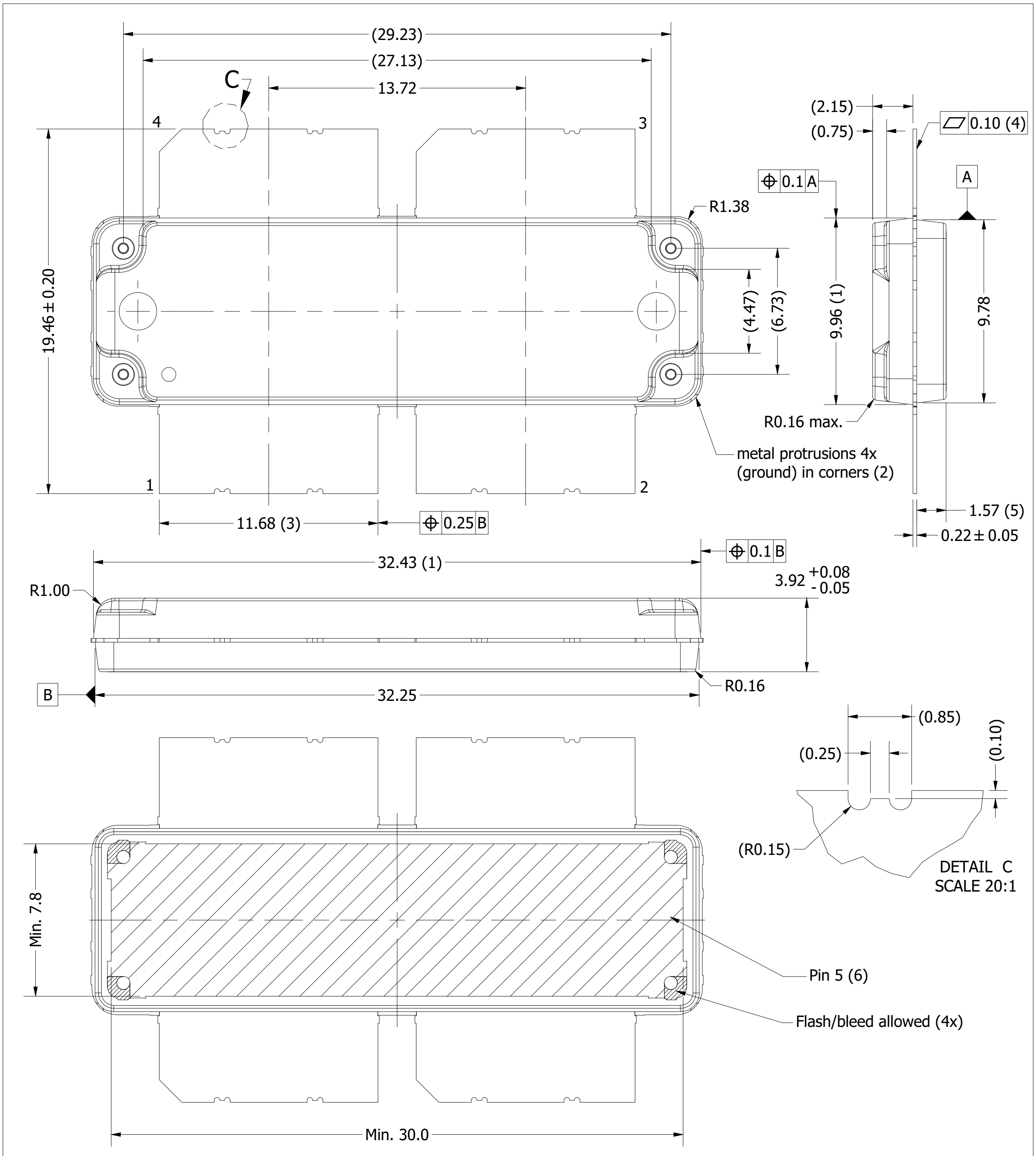
(5) V_{DS} = 40 V

(6) V_{DS} = 30 V

Fig 10. Drain efficiency as a function of output power; typical values

8. Package outline

OMP-1230-4F-1

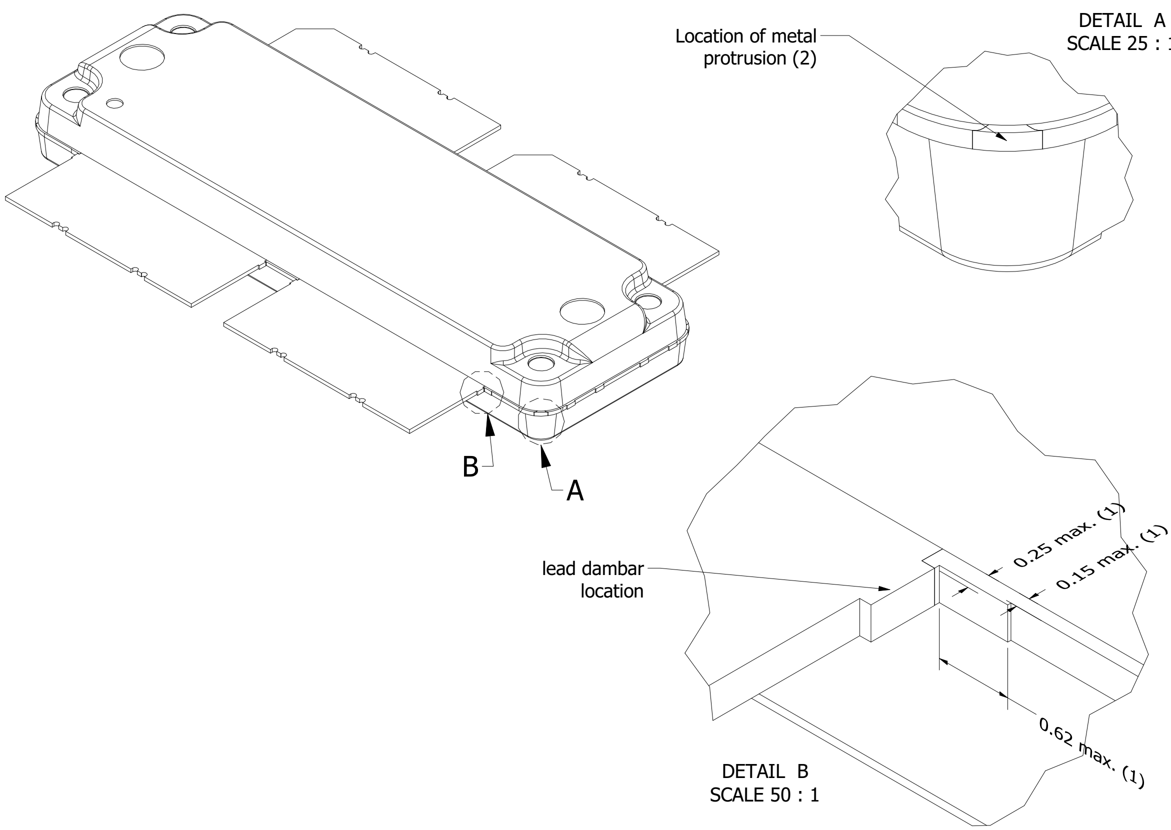


Package outline drawing: OMP-1230-4F-1	units in mm.	Tolerances unless otherwise stated: Dimension: ± 0.05 Angle: ± 1°	Revision: 0 Revision date: 7/2/2019
		Third angle projection	Sheet 1 of 2

Fig 11. Package outline OMP-1230-4F-1 (sheet 1 of 2)

OMP-1230-4F-1

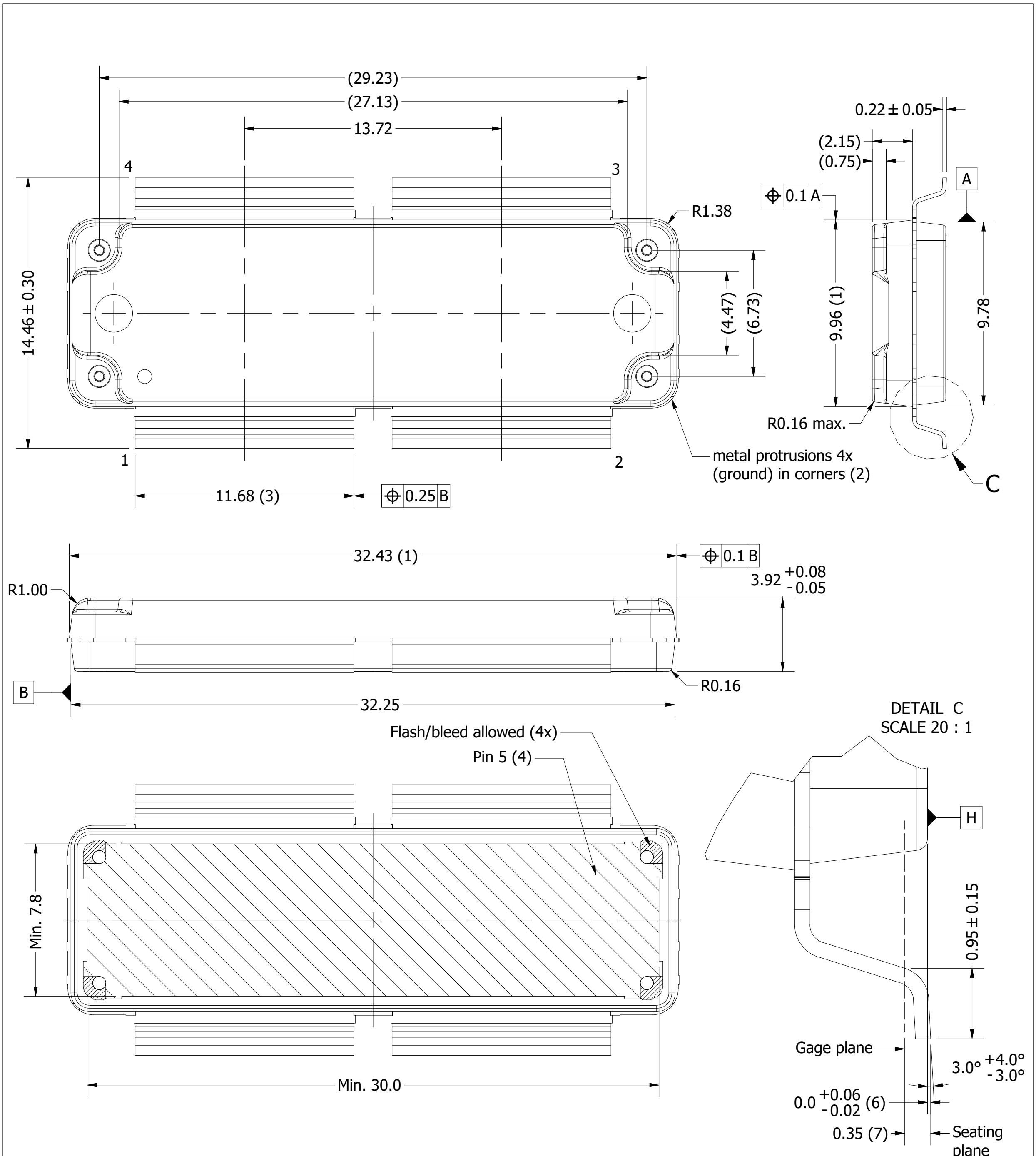
Drawing Notes	
Items	Description
(1)	Dimensions are excluding mold protrusion. All areas located adjacent to the leads have a maximum mold protrusion of 0.25 mm (per side) and max. 0.62 mm in length. At all other areas the mold protrusion is maximum 0.15 mm per side. See also detail B.
(2)	The metal protrusion (tie bars) in the corner will not stick out of the molding compound protrusions (detail A).
(3)	The lead dambar (metal) protrusions are not included. Add 0.14 mm max to the total lead dimension at the dambar location.
(4)	The lead coplanarity over all leads is 0.1 mm maximum.
(5)	Dimension is measured from bottom of lead to bottom of plastic package. Dimension is measured 0.5 mm from the edge of the package body.
(6)	The hatched area indicates the exposed metal heatsink.
(7)	The leads and exposed heatsink are plated with matte Tin (Sn).



Package outline drawing: OMP-1230-4F-1	units in mm.	Tolerances unless otherwise stated: Dimension: ± 0.05 Angle: ± 1°	Revision: 0 Revision date: 7/2/2019
		Third angle projection	Sheet 2 of 2

Fig 12. Package outline OMP-1230-4F-1 (sheet 2 of 2)

OMP-1230-4G-1

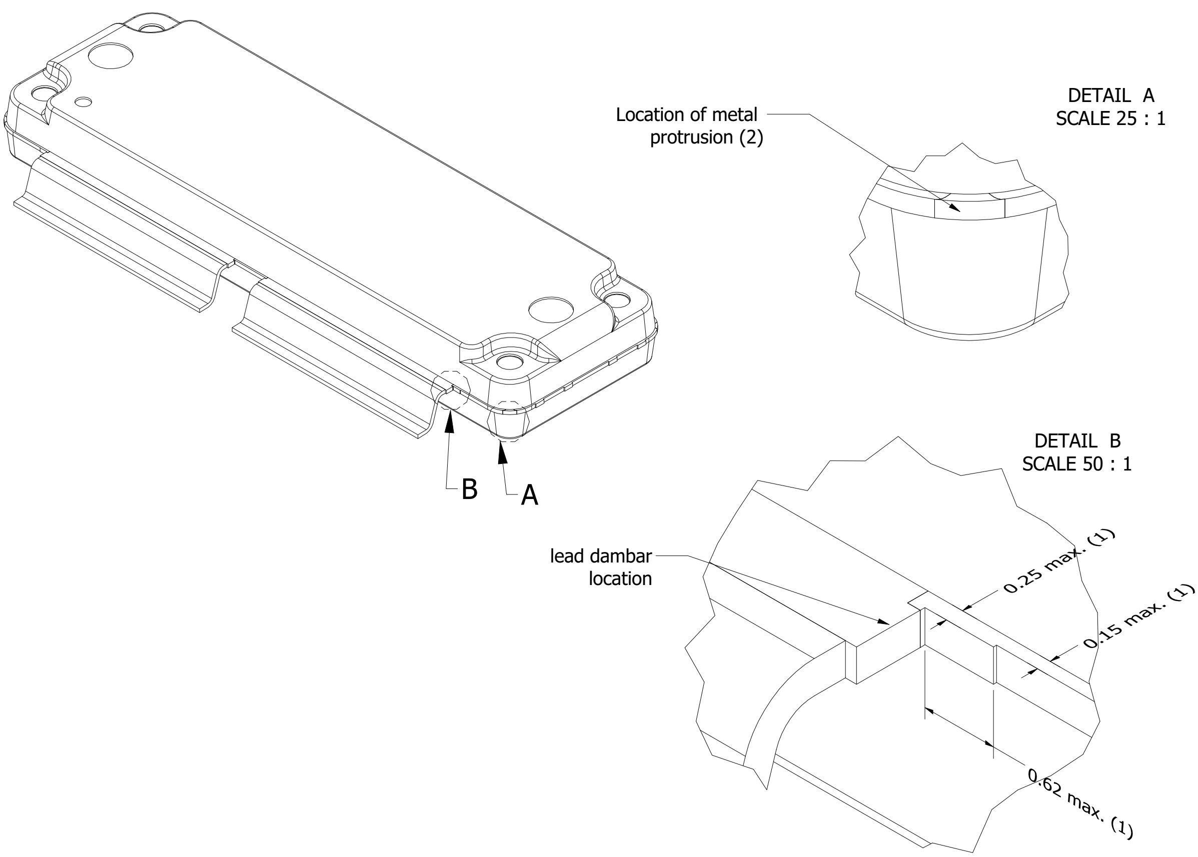


Package outline drawing: OMP-1230-4G-1	units in mm.	Tolerances unless otherwise stated: Dimension: ± 0.05 Angle: ± 1°	Revision: 0 Revision date: 7/2/2019
		Third angle projection	Sheet 1 of 2

Fig 13. Package outline OMP-1230-4G-1 (sheet 1 of 2)

OMP-1230-4G-1

Drawing Notes	
Items	Description
(1)	Dimensions are excluding mold protrusion. Areas located adjacent to the leads have a maximum mold protrusion of 0.25 mm (per side) and 0.62 mm max. in length. At all other areas the mold protrusion is maximum 0.15 mm per side. See also detail B.
(2)	The metal protrusion (tie bars) in the corner will not stick out of the molding compound protrusions (detail A).
(3)	The lead dambar (metal) protrusions are not included. Add 0.14 mm max to the total lead dimension at the dambar location.
(4)	The hatched area indicates the exposed metal heatsink.
(5)	The leads and exposed heatsink are plated with matte Tin (Sn).
(6)	Dimension is measured with respect to the bottom of the plastic package Datum H. Positive value means that the bottom of the package is higher than the bottom of the lead.
(7)	Gage plane (foot length) to be measured from the seating plane.



Package outline drawing: OMP-1230-4G-1	units in mm.	Tolerances unless otherwise stated: Dimension: ± 0.05 Angle: ± 1°	Revision: 0 Revision date: 7/2/2019
		Third angle projection	Sheet 2 of 2

Fig 14. Package outline OMP-1230-4G-1 (sheet 2 of 2)

9. Handling information

CAUTION	
	This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices. Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

Table 11. ESD sensitivity

ESD model	Class
Charged Device Model (CDM); According to ANSI/ESDA/JEDEC standard JS-002	C2A
Human Body Model (HBM); According to ANSI/ESDA/JEDEC standard JS-001	2

10. Abbreviations

Table 12. Abbreviations

Acronym	Description
CW	Continuous Wave
ESD	ElectroStatic Discharge
FM	Frequency Modulation
ISM	Industrial, Scientific and Medical
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
MRI	Magnetic Resonance Imaging
RoHS	Restriction of Hazardous Substances
SMD	Surface Mounted Device
UHF	Ultra High Frequency
VHF	Very High Frequency
VSWR	Voltage Standing Wave Ratio

11. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
ART2K0PE_ART2K0PEG v.5	20240807	Product data sheet	-	ART2K0PE_ART2K0PEG v.4
Modifications:	• Table 10 on page 6: changed value row C8			
ART2K0PE_ART2K0PEG v.4	20230907	Product data sheet	-	ART2K0PE_ART2K0PEG v.3
ART2K0PE_ART2K0PEG v.3	20201019	Product data sheet	-	ART2K0PE v.2
ART2K0PE v.2	20200806	Product data sheet	-	ART2K0PE_ART2K0PEG v.1
ART2K0PE_ART2K0PEG v.1	20200114	Objective data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.ampleon.com.

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Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

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13. Contact information

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14. Contents

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