CA-234-14

BLF882 at 470-705 MHz

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AMPLEON

Application Measurement Report

Document information

Info	Content
Keywords	CA-234-14
Abstract	Measurement results of a BLF882 device at 470-705MHz with an output power of 33W Avg. DVB-T or ISDB-T.

Revision history

Rev	Date	Description
1	20140902	Initial version
2	20141111	Updated Para.1.4
3	20150128	Misc. updates
4	20150424	Update for web publication
5	20151005	The format of this document has been redesigned to comply with the new identity guidelines of Ampleon. Legal texts have been adapted to the new company name where appropriate.

1. Information

1.1 General Description

This document contains measurement results of a BLF882 device from 470 to 705 MHz tested with a DVB-T signal. This application board was optimized at 50Vds for P3dB >200W pulsed CW and 30-33W avg. DVB-T with maximum efficiency while still meeting >8dB PAR. Test report CA-213-14 is available and shows a BLF882 application board optimized at a lower supply voltage and lower peak power for maximum efficiency at 22W avg. DVB-T and 8dB PAR. For maximize efficiency the device needs to operate at as high as possible average DVB-T output power and still meet the linearity PAR requirements.

1.2 Test object details

Transistor type: BLF882 (screwed down with Berquist TIC4000 thermal and elec. conductive paste)

Production code: D141471

Package: SOT502A3

Board: 30 mil thick, RF35

Demo number: 2872

1.3 Test Setup

Test Signal: DVB-T & CW Load: Bird 1kW, 30dB, Aeroflex/Weinschel 82-30-34

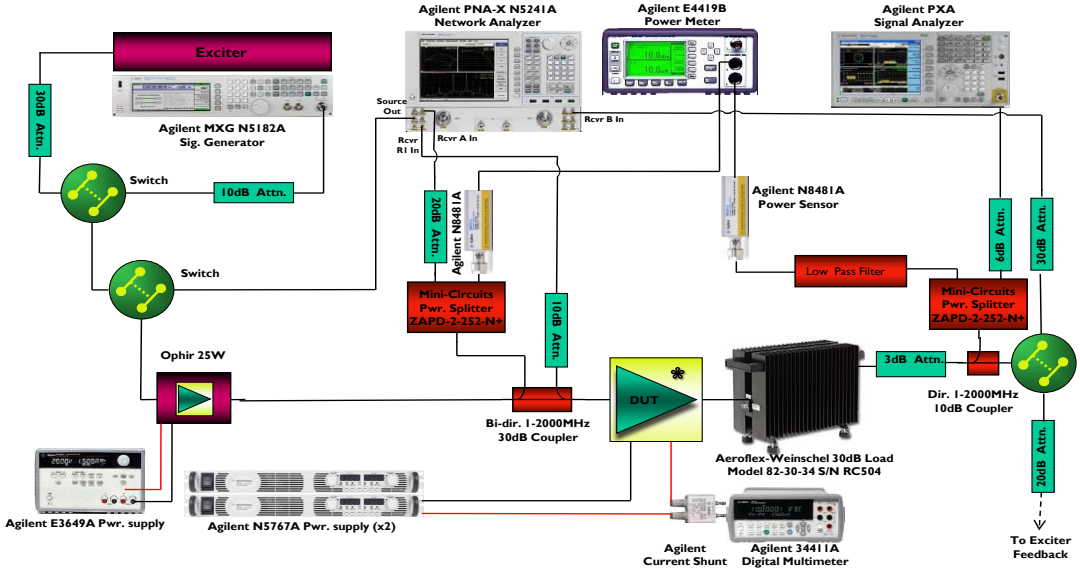

Fig 1. Test Setup → See Fig 8 for connections to DUT

1.4 Typical Performance BLF882

Symbol	Parameter	470-705 MHz	470-705 MHz	Unit
V_{DS}	Power supply	**50**	**50**	mA
I_{Dq}	Quiescent current	210	210	V
Pout	Avg. DVB-T Output Power	**30**	**33**	W
G_{min}	Min. Gain	20.7	20.6	dB
$G_{flatness}$	Gain flatness	2.0	2.1	dB
Eff.	Efficiency	26.4-29.5	27.7-30.9	%
PAR	PAR	8.3 – 8.6	8.0 – 8.4	dB
P3dB	Peak Pulsed (50usec PW, 10%)	53.3 – 53.4 212 - 221	53.3 – 53.4 212 - 221	dBm W

2. Summary

This document contains measurement results of a BLF882 device from 470 to 705MHz tested with a DVB-T signal. This application board was optimized at 50Vds for P3dB >200W pulsed CW and 30W avg. DVB-T (26.5-29.5% eff.) and 33W avg. DVB-T (27.7-30.9% eff.) while still meeting >8dB PAR. Test report CA-213-14 is available and shows a BLF882 application board optimized at a lower supply voltage and lower peak power for maximum efficiency at 22W avg. DVB-T and 8dB PAR. Note: to maximize efficiency the device needs to operate at as high as possible average DVB-T output power while still meeting the linearity PAR requirements.

3. Measurement Results

3.1 DVB-T

3.1.1 PAR at 30W and 33W Average DVB-T Output power (50Vds).

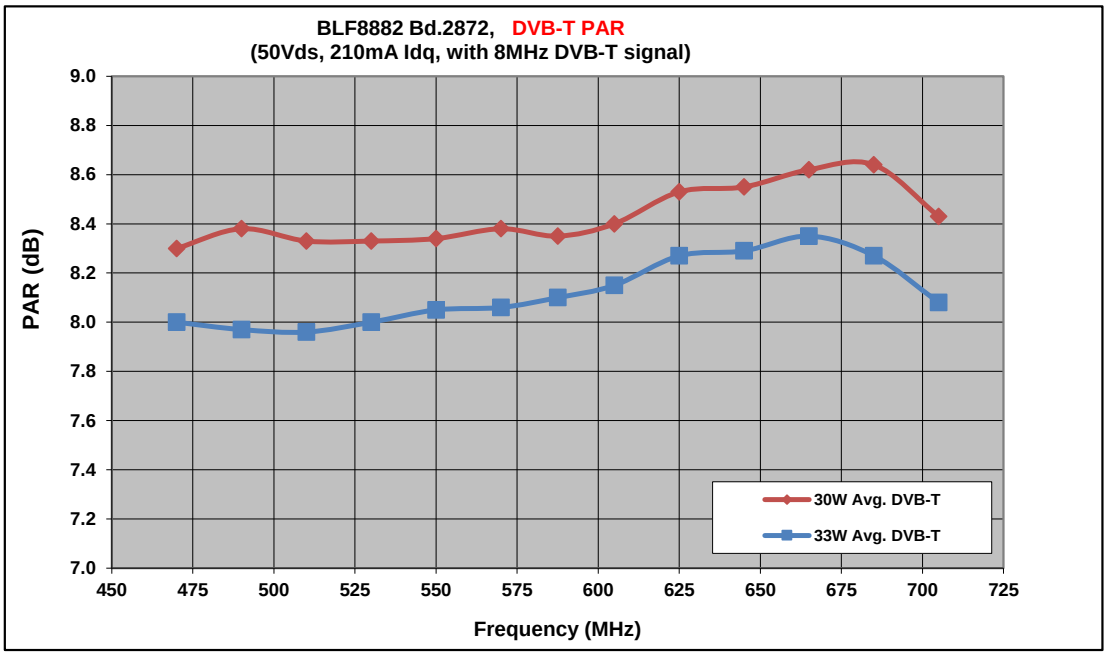

Fig 2. PAR at 30W & 33W avg. DVB-T

3.1.2 Efficiency at 30W & 33W avg. DVB-T output power (50Vds).

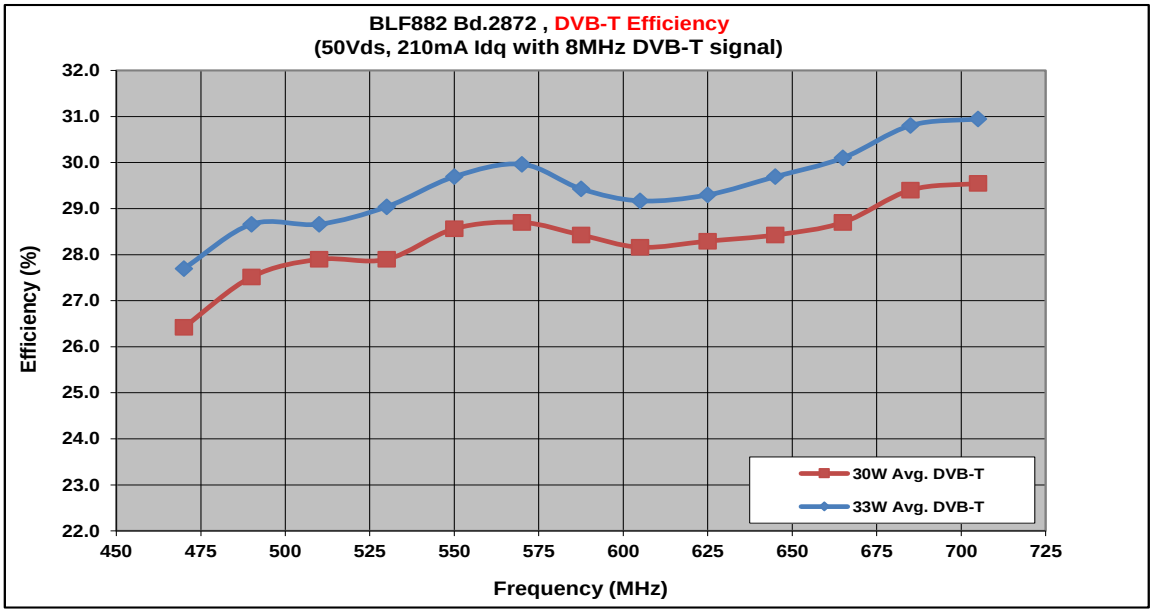

Fig 3. Efficiency at 30W & 33W avg. DVB-T

3.1.3 Gain at 30W & 33W avg. DVB-T output power (50Vds).

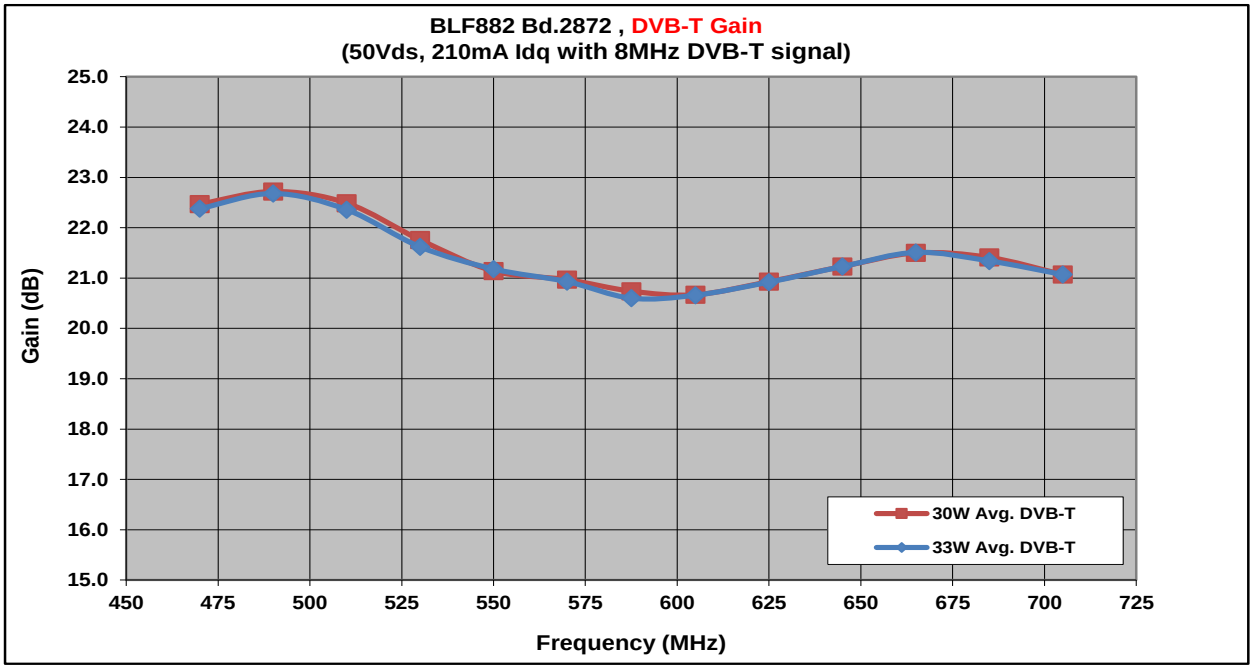

Fig 4. Gain at 30W & 33W avg. DVB-T

3.1.4 Data for DVB-T

Meas. Results with 8MHz DVB-T signal @ 30W avg. DVB-T Output Power and Vds=50V, 210mA Idq									
Frequency	Vds	Idq	Pin	Pout		Gain	Id1	Eff	PAR
(MHz)	(V)	(A)	(dB)	(dB)	(W)	(dB)	(A)	(%)	(dB)
470	50	0.210	22.30	44.77	30.0	22.5	2.270	26.4	8.3
490	50	0.210	22.05	44.77	30.0	22.7	2.180	27.5	8.4
510	50	0.210	22.28	44.77	30.0	22.5	2.150	27.9	8.3
530	50	0.210	23.01	44.77	30.0	21.8	2.150	27.9	8.3
550	50	0.210	23.63	44.77	30.0	21.1	2.100	28.6	8.3
570	50	0.210	23.80	44.77	30.0	21.0	2.090	28.7	8.4
587.5	50	0.210	24.03	44.77	30.0	20.7	2.110	28.4	8.4
605	50	0.210	24.10	44.77	30.0	20.7	2.130	28.2	8.4
625	50	0.210	23.84	44.77	30.0	20.9	2.120	28.3	8.5
645	50	0.210	23.54	44.77	30.0	21.2	2.110	28.4	8.6
665	50	0.210	23.27	44.77	30.0	21.5	2.090	28.7	8.6
685	50	0.210	23.36	44.77	30.0	21.4	2.040	29.4	8.6
705	50	0.210	23.70	44.77	30.0	21.1	2.030	29.5	8.4

Table 1. DVB-T data at 30W avg. DVB-T

Meas. Results with 8MHz DVB-T signal @ 33W avg. DVB-T Output Power and Vds=50V, 210mA Idq									
Frequency	Vds	Idq	Pin	Pout		Gain	Id1	Eff	PAR
(MHz)	(V)	(A)	(dB)	(dB)	(W)	(dB)	(A)	(%)	(dB)
470	50	0.210	22.80	45.18	33.0	22.4	2.380	27.7	8.0
490	50	0.210	22.50	45.18	33.0	22.7	2.300	28.7	8.0
510	50	0.210	22.82	45.18	33.0	22.4	2.300	28.7	8.0
530	50	0.210	23.56	45.18	33.0	21.6	2.270	29.0	8.0
550	50	0.210	24.00	45.18	33.0	21.2	2.220	29.7	8.1
570	50	0.210	24.25	45.18	33.0	20.9	2.200	30.0	8.1
587.5	50	0.210	24.58	45.18	33.0	20.6	2.240	29.4	8.1
605	50	0.210	24.52	45.18	33.0	20.7	2.260	29.2	8.2
625	50	0.210	24.26	45.18	33.0	20.9	2.250	29.3	8.3
645	50	0.210	23.95	45.18	33.0	21.2	2.220	29.7	8.3
665	50	0.210	23.67	45.18	33.0	21.5	2.190	30.1	8.4
685	50	0.210	23.84	45.18	33.0	21.3	2.140	30.8	8.3
705	50	0.210	24.11	45.18	33.0	21.1	2.130	30.9	8.1

Table 2. DVB-T data at 33W avg. DVB-T

3.2 Pulsed CW Sweeps

3.2.1 Pulsed Peak Power & Efficiency as a function of Output Power. (50us pw/10%)

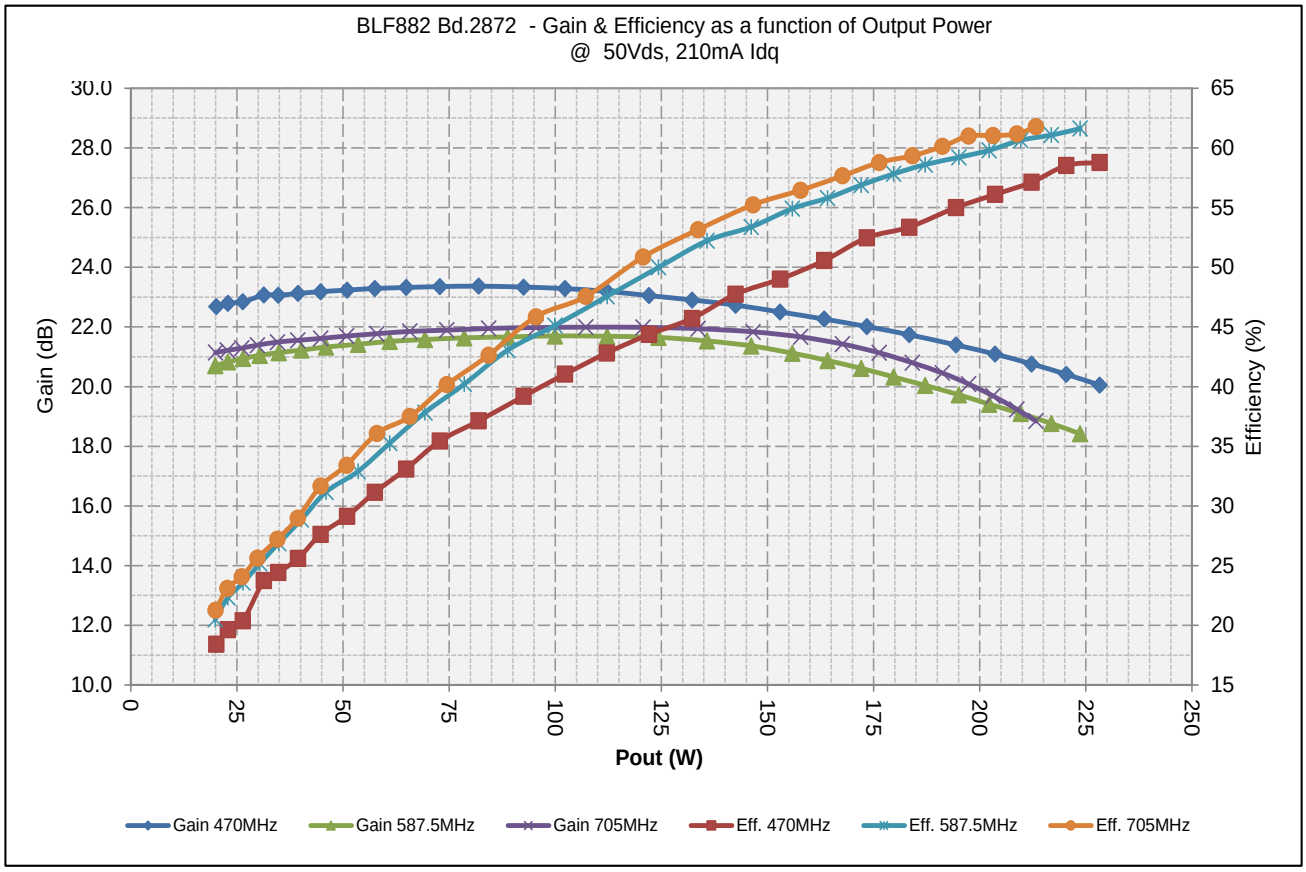

Fig 5. Pulsed Peak Power & Efficiency

3.3 CW – Network Analyzer Sweep

3.3.1 Gain & Input Return Loss at approx. 22W CW, 42Vds

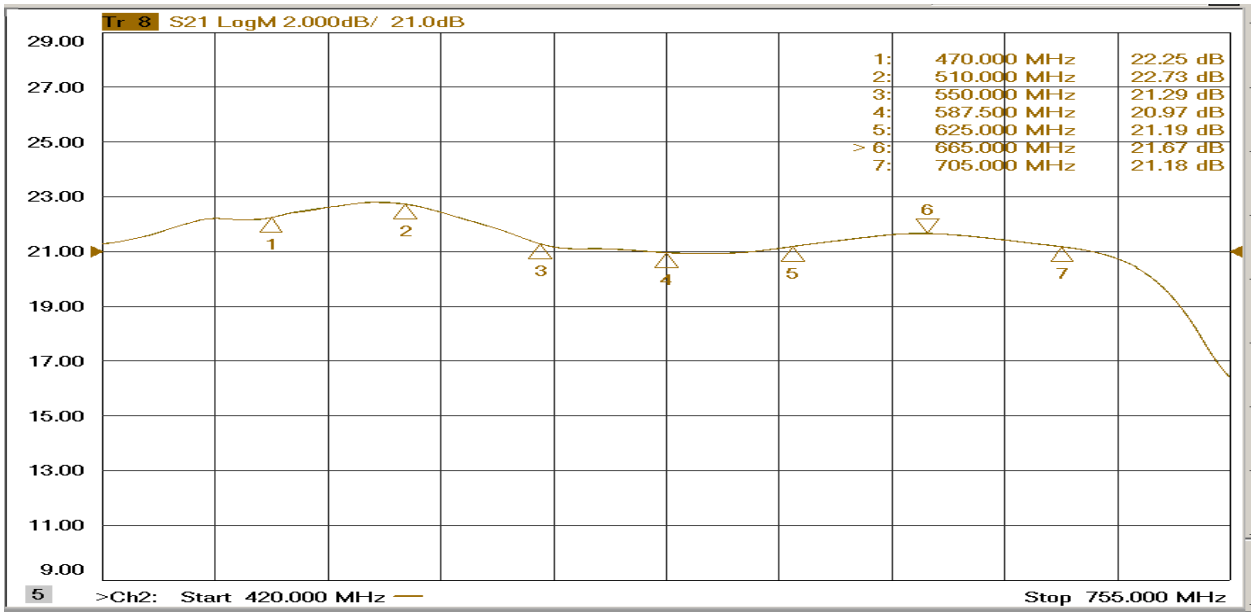

Fig 6. Gain as a function frequency. (@ approx. 30W CW)

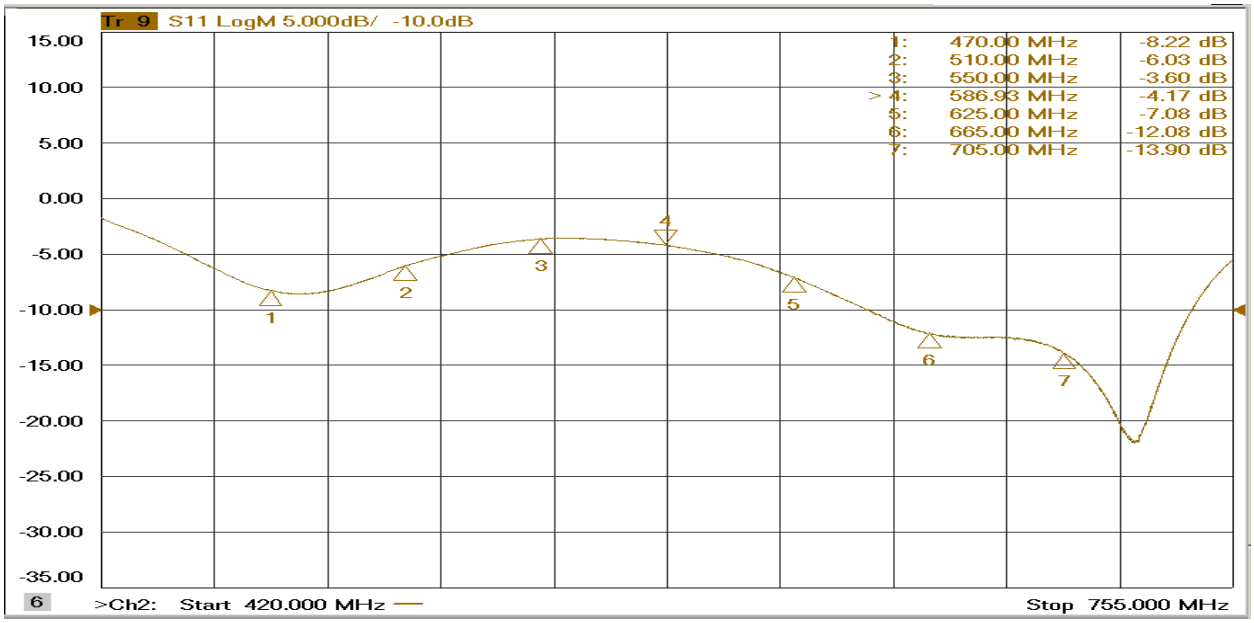

Fig 7. Return Loss as a function frequency. (@ approx. 30W CW)

3.4 Harmonics

3.4.1 Maximum Harmonics for Pulsed CW Sweep

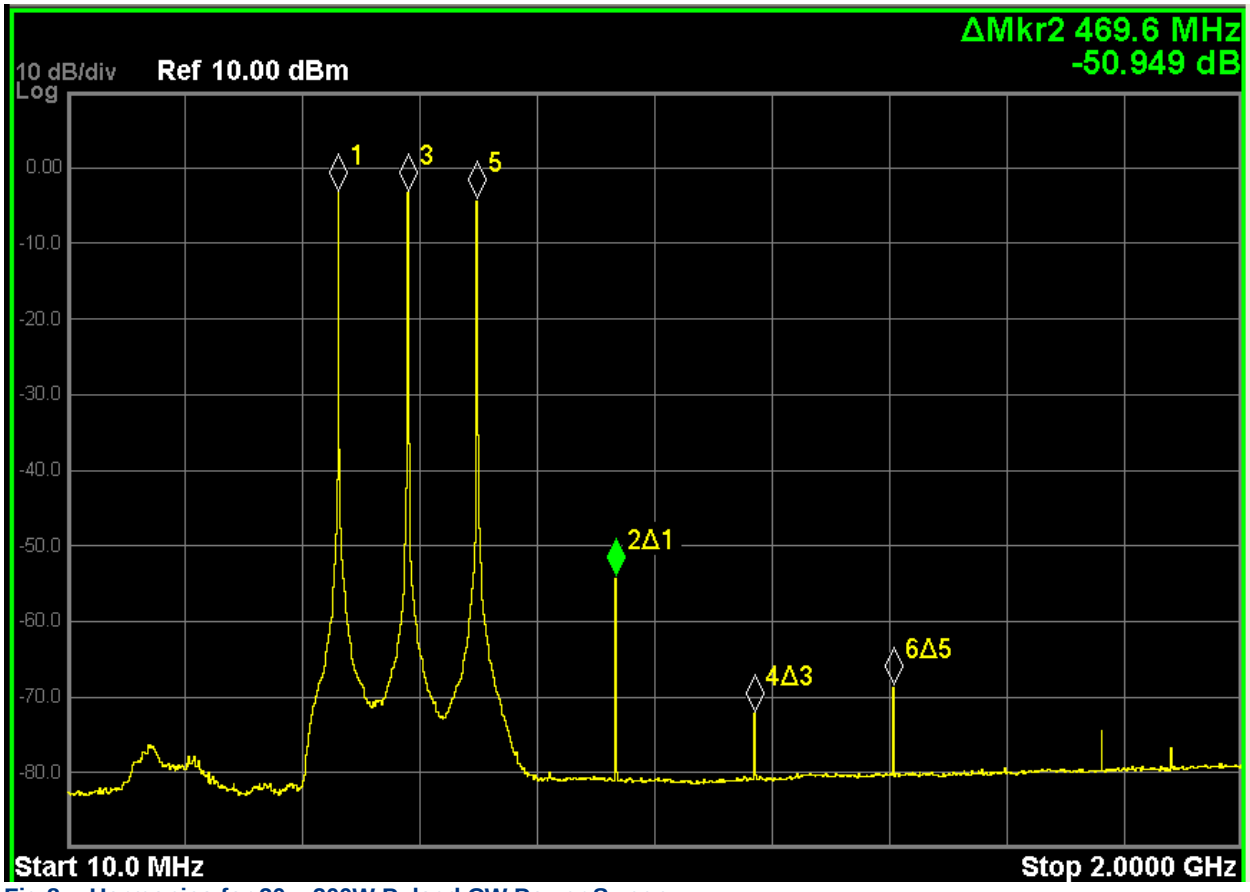

Fig 8. Harmonics for 20 – 200W Pulsed CW Power Sweep

4. Photo

4.1 Application Circuit Connections

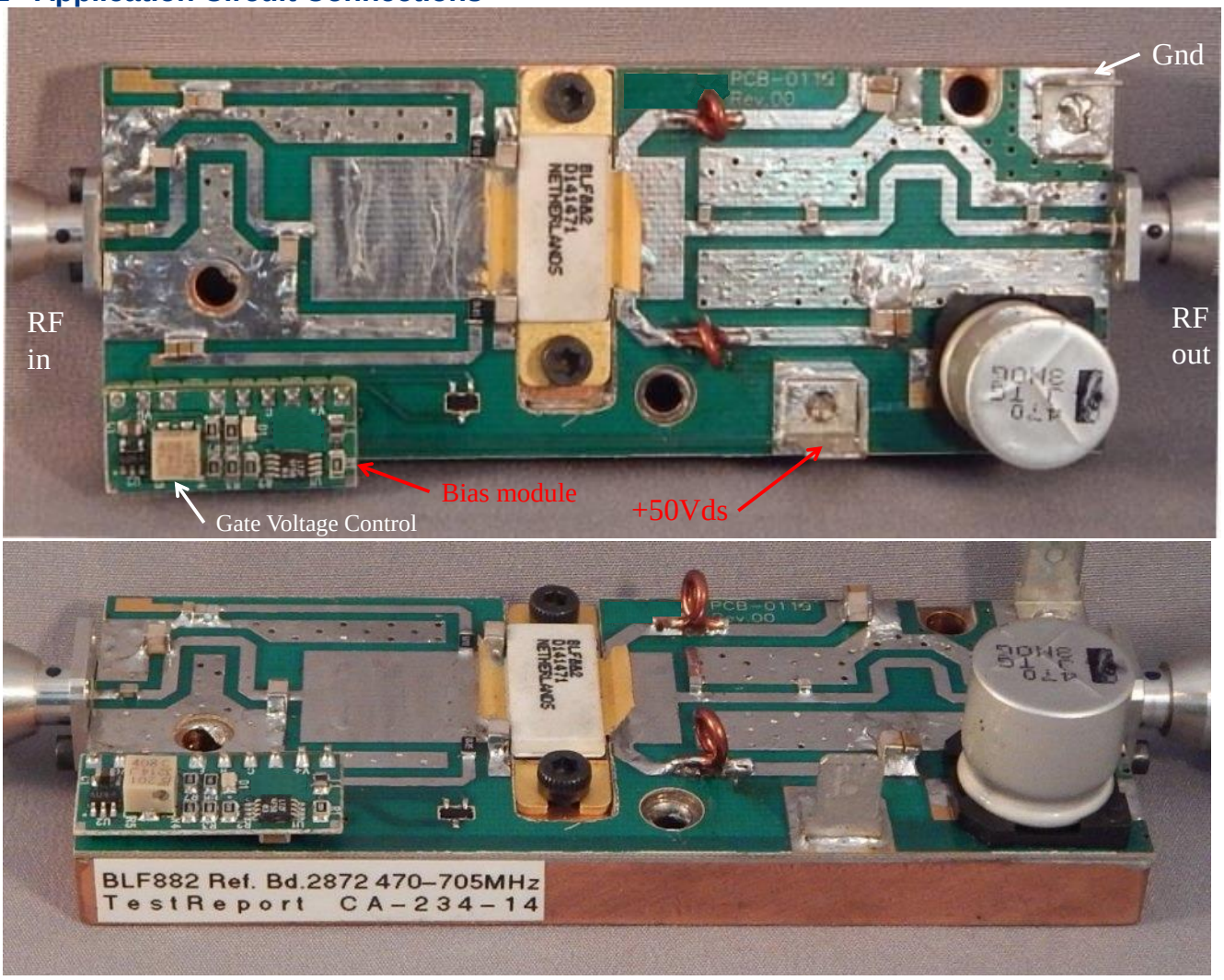

Fig 9. BLF882 Bd.#2872

This amplifier requires a 50V DC power supply connected to the Vds input shown above. This power supply is used for both the drain supply and for our LDMOS bias module which supplies the gate voltage. Details of the LDMOS bias module are in **R_10032 (CA-330-11)**. RF input is connected to the N-type connector on the left and the amplifier load is connected to the RF output N-type connector on the right.

5. Layout and Material List

5.1 Layout

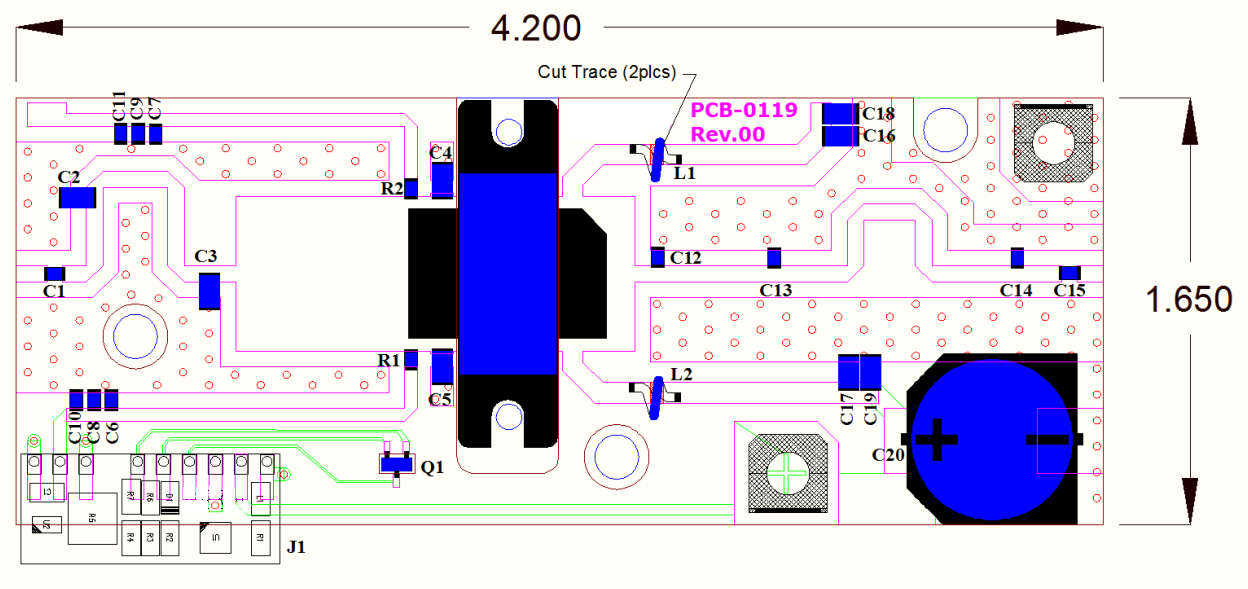

Fig 10. Layout (AutoCAD dxf file attached)

5.2 Material List

Designator	Description	Manufacturer	Part #
PCB	PCB 30 mil Thick, Taconics RF35	Avanti Circuits	PCB0119 Rev.00
Base Plate	1pc. Copper pallet	Jones Machine	SMI0068 Rev.0
Q1	2N2222 NPN Transistor	Fairchild	MMBT2222
Q2	BLF882	Ampleon	BLF882
R1, R2	5.1Ω, 1206		
L1, L2	1 T Coil, 16awg, 0.125 ID		
C1	56 pF	Passive Plus	0805N
C2	9.1 pF *	Passive Plus	1111N
C3	27 pF *	Passive Plus	1111N
C4	24 pF *	Passive Plus	1111N
C5	24 pF *	Passive Plus	1111N
C6	82 pF	Passive Plus	0805N
C7	82 pF	Passive Plus	0805N
C8	100nF 50V 10% X7R 0805	Multicomp	U0805W104K1HRN-P4
C9	100nF 50V 10% X7R 0805	Multicomp	U0805W104K1HRN-P4
C10	10uF Capacitor, 10V 10%X5R, 0805	Murata	GRM21BR61A106KE19L
C11	10uF Capacitor, 10V 10%X5R, 0805	Murata	GRM21BR61A106KE19L
C12	27 pF	Passive Plus	0805N
C13	18 pF	Passive Plus	0805N
C14	5.6 pF	Passive Plus	0805N
C15	56 pF	Passive Plus	0805N
C12	1000 pF	Passive Plus	0805N
C16, C17	82 pF *	Passive Plus	1111N
C18, C19	0.1uF 250V 10% X7R 1206 *	Murata	GRM32DR72E104KW01L
C20	470 uF, 63V electrolytic, SMD		
***Capacitor mounted on narrow side.**			

Table 3. BLF882 Material List

6. Copper Base Plate

6.1 Base plate

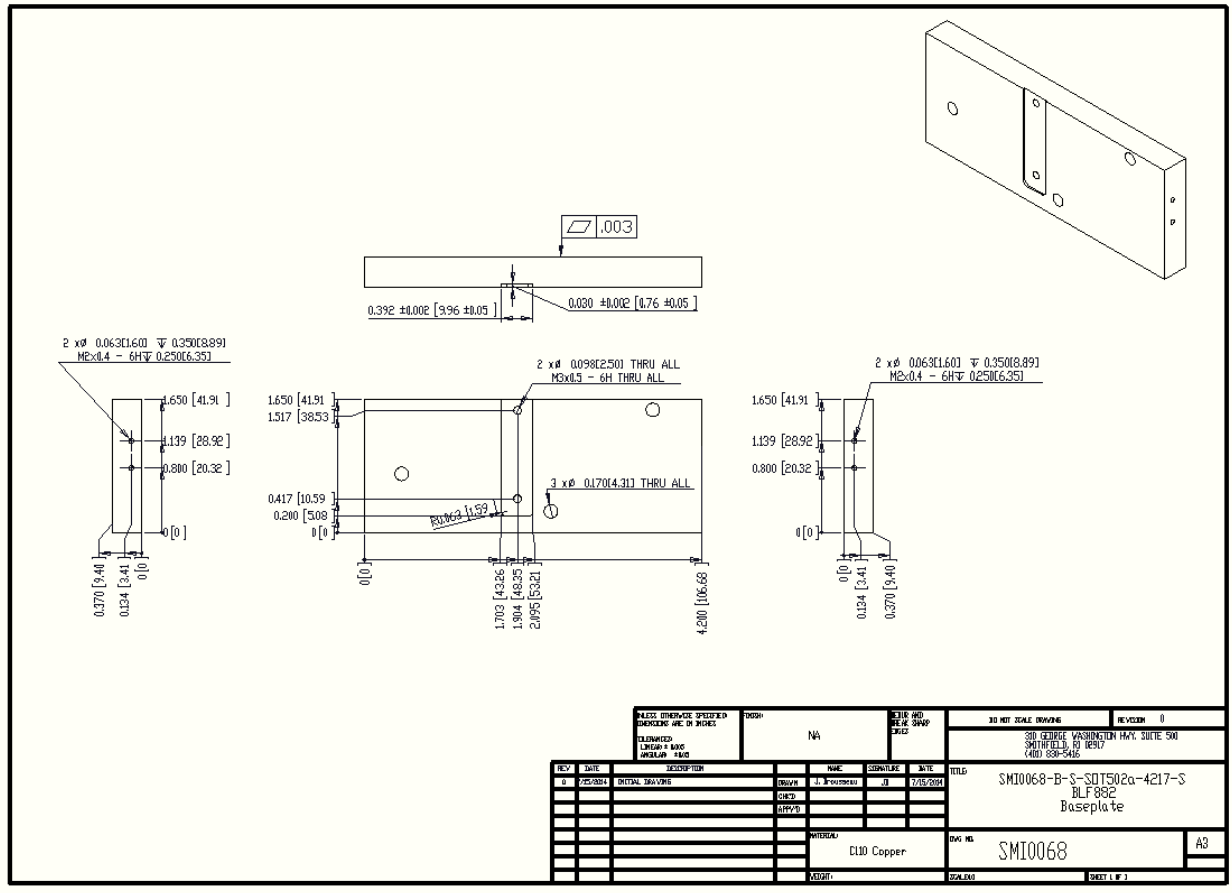

Fig 11. Base Plate drawing (AutoCAD dxf file attached)

7. DVB-T Signal

7.1 DVB-T Signal CCDF

Using MXG N5182A and Agilent PXA

Parameter	PXA
0.01% CCDF (dB)	9.7
Resolution BW	10.000 MHz
Counts (or Points)	10.0 Mpts
Attenuation	Auto

8. Attachments

Please see the attachment for the support files.

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