

AR201207

BLP05H9S500P, 433 MHz

v1.0 – September 25, 2020

AMPLEON

Application Report

Document information

Status	v1.0
Abstract	Measurement results of a demoboard design for the BLP05H9S500P optimized for 500W, 433 MHz.
Demo Number	AR201207

1. Revision History

Table 1 – Report revisions

Revision	Date	Description	Author
1.0	2020.09.25	Initial document	

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5. General Description

This report presents the measurement results of the high efficiency 500W GEN 9 High Voltage LDMOS transistor, namely BLP05H9S500P, at 433 MHz.

Measurements have been performed on a dedicated demo-circuit, matched to 50 Ω at input and output. Transistor and PCB have been soldered during assembly.

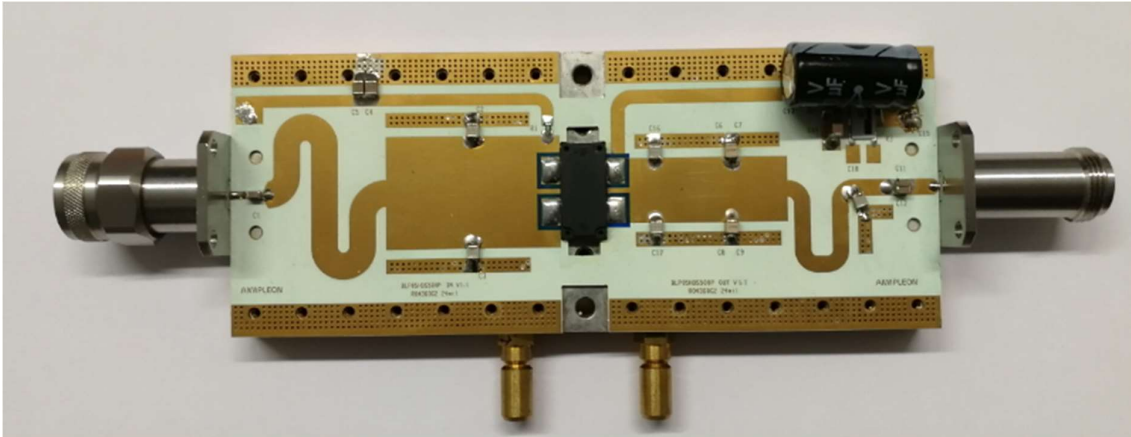


Figure 1 – Demo front view

Table 2 – Test circuit information

Parameter	Description	Unit
Input Laminate Type	Rogers RO4360G2	
Output Laminate Type	Rogers RO4360G2	
Laminate thickness	0.61	mm
Overall dimensions	150 x 60	mm
Cooling type	Indirect water cooling	
Device Package	SOT1223-2	

6. CW RF characteristics

Table 3 – Performance indication

Test signal: CW; RF performance at $V_{DS}=50V$; $I_{Dq}=50mA$; $T_{cooling\ water}=25^{\circ}C$

Symbol	Parameter	Conditions	Typical	Unit
f	Frequency		433	MHz
V_{DS}	Drain-source voltage		50	V
V_{GS}	Gate-source voltage	$I_{Dq} = 50mA$	1.77	V
G_p	Power gain	$P_{1dBcp} = 514.87W$	25.3	dB
η_D	Drain efficiency	$P_{1dBcp} = 514.87W$	75.08	%

7. CW Performance Details

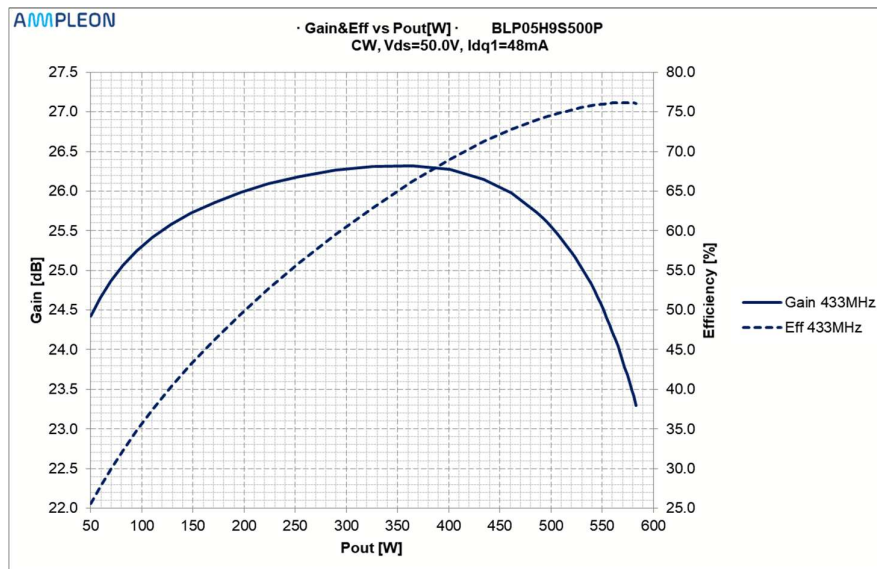


Figure 2 – BLP05H9S500P demo board CW performance

Table 4 – RF Performance overview

Freq [MHz]	Gmax [dB]	Pout@Gmax [W]	P1dB [W]	P2dB [W]	P3dB [W]	Effmax [%]	Pout@Effmax [W]	Eff P1dB [%]	Eff P2dB [%]	Eff P3dB [%]
433	26.32	364.05	514.87	557.26	582.45	76.14	574.47	75.08	76.07	76.09

8. User Guide

8.1 Biasing

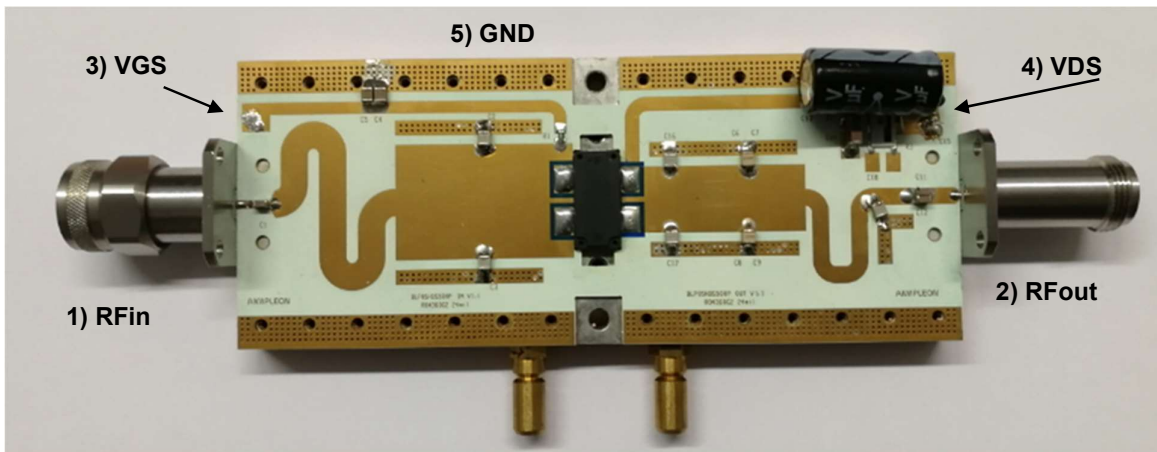


Figure 3 – BLP05H9S500P application board pin configuration

Table 5 – Pin description

Symbol	Pin	Description
RF _{IN}	1	RF input
RF _{OUT}	2	RF output
V _{GS}	3	Gate-source voltage
V _{DS}	4	Drain-source voltage
GND	5	Negative supply terminal for V _{DS} and V _{GS} respectively

8.2 Bill of Materials

Table 6 – Bill of Materials

Part	Description	Part number	Value/Remark
C1,C4,C11,C12,C13	Multilayer ceramic chip capacitor	270 pF	ATC800B
C2, C3	Multilayer ceramic chip capacitor	75 pF	ATC800B
C6, C8	Multilayer ceramic chip capacitor	43 pF	ATC800B
C7, C9			Not present
C10	Multilayer ceramic chip capacitor	12 pF	ATC800B
C16, C17	Multilayer ceramic chip capacitor	16 pF	ATC800B
C5, C14	Multilayer ceramic chip capacitor	4.7uF / 100V	C3225X7S2A475K200AE
C15	Electrolytic capacitor	470 uF/63V	MAL203858471E3
R1	Chip resistor	10R	0806
R2, R4	Chip resistor	9.1R	1206
Rx (optional)	Shunt resistor	Ohmite\FC4L110R010FER	0.01Ω
T1	LDMOS transistor	BLP05H9S500P	Ampleon
Input PCB	Rogers RO4360G2		24 mil thickness
Output PCB	Rogers RO4360G2		24 mil thickness

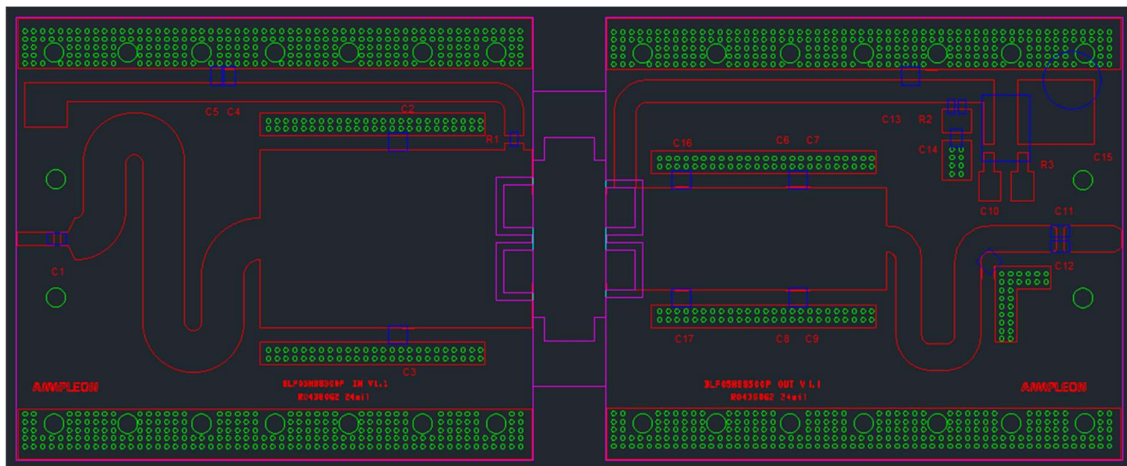


Figure 4 – BLP05H9S500P application board components description

8.3 Temperature behavior

For operation of this demo board water cooling should be applied.
Water temperature should be kept below 65 °C.

8.4 Device markings

Table 7 – Module specifics

Parameter	Value
Manufacturer	Ampleon
Device	BLP05H9S500P
Comments	Engineering sample

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