

# AR191206

BLF0910H9LS750P  
902-928 MHz, 750W

v1.0 – April 09, 2019

AMPLEON

Application Report

## Document information

**Status** v1.0

**Abstract** Measurement results of a demoboard design with the BLF0910H9LS750P in the 902-928 MHz bandwidth

## 1. Revision History

Table 1 – Report revisions

| Revision | Date       | Description      | Author |
|----------|------------|------------------|--------|
| 1.0      | 2019.04.09 | Initial document |        |

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## 5. General description

This report presents the measurement results of the demoboard designed for the 902-928 MHz frequency band using the high-efficiency BLF0910H9LS750P transistor based on GEN 9 HV LDMOS technology. During the assembly, PCB and transistor have been soldered to the baseplate.

The dedicated demo-circuit is matched to 50 Ω at input and output.

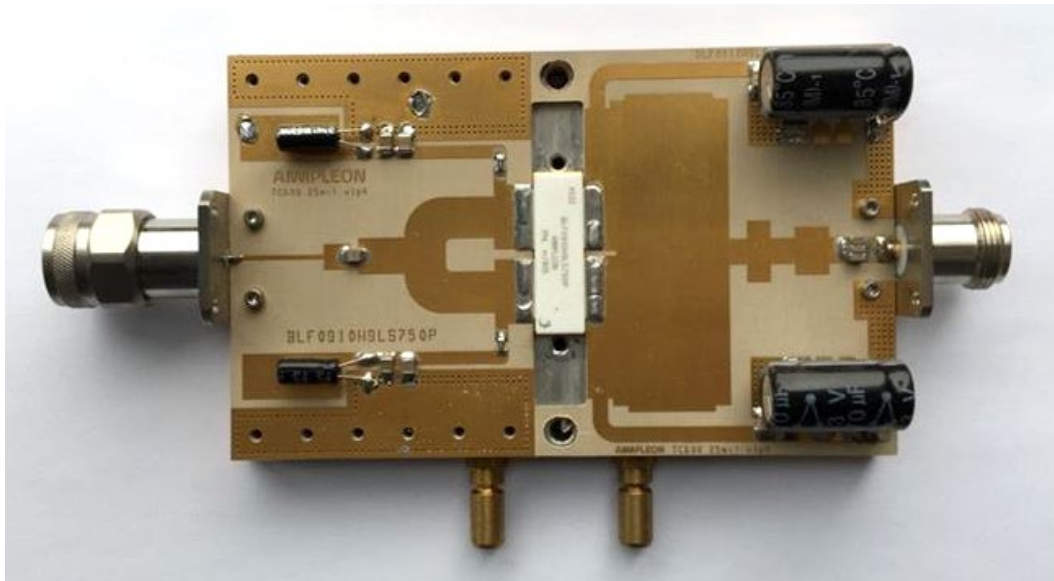


Figure 1 – Demo front view

Table 2 – Test circuit information

| Parameter          | Description            | Unit |
|--------------------|------------------------|------|
| Laminate Type      | TC600                  |      |
| Dk                 | 6.15                   |      |
| Df                 | 0.002 @10 GHz          |      |
| Laminate thickness | 0.635                  | mm   |
| Overall dimensions | 130.3 x 80             | mm   |
| Cooling type       | Indirect water cooling |      |
| Device Package     | SOT539B                |      |

## 6. CW RF characteristics

Table 3 – Performance indication

Test signal: CW, RF performance at  $V_{DS}=50V$ ;  $I_{Dq}=100mA$ ;  $T_{cooling\ water}=25^{\circ}C$

| Symbol   | Parameter            | Conditions                     | Typical | Unit |
|----------|----------------------|--------------------------------|---------|------|
| f        | Frequency            |                                | 915     | MHz  |
| $V_{DS}$ | Drain-source voltage |                                | 50      | V    |
| $V_{GS}$ | Gate-source voltage  | $I_{Dq} = 50mA \times section$ | 1.9     | V    |
| $G_p$    | Power Gain           | $P_{2dBcp} = 850.5W$           | 20.8    | dB   |
| $\eta_D$ | Drain Efficiency     | $P_{2dBcp} = 850.5W$           | 70.8    | %    |

## 7. CW Performance Details

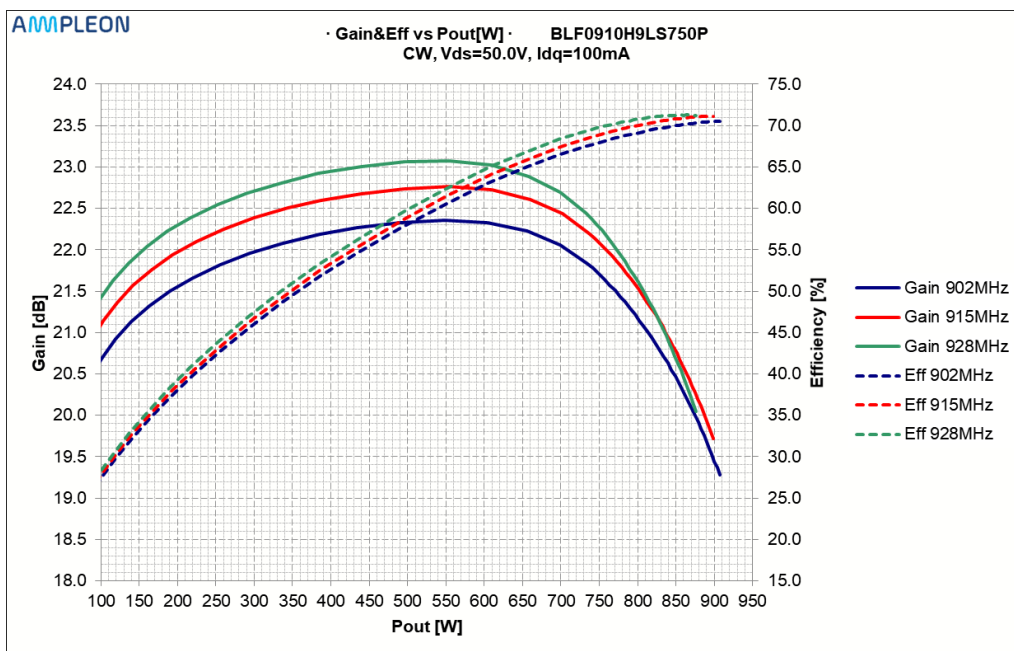


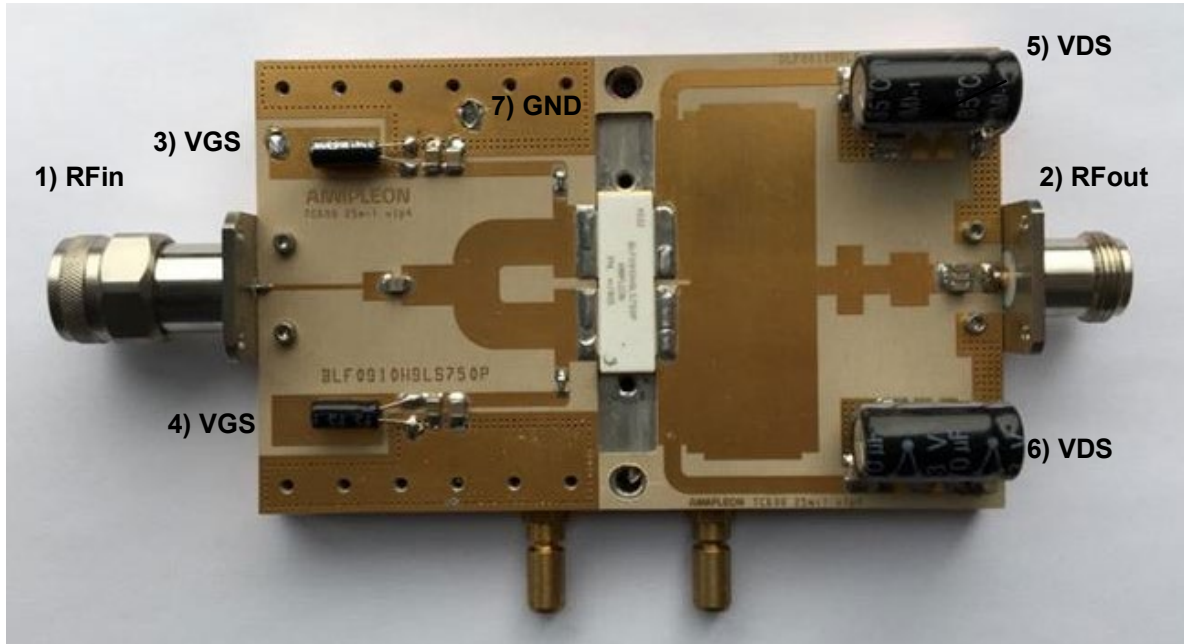
Figure 2 – Demo board CW performance

Table 4 – RF Performance overview

| Freq [MHz] | Gmax [dB] | Pout@Gmax [W] | P1dB [W] | P2dB [W] | P3dB [W] | Effmax [%] | Pout@Effmax [W] | Eff P1dB [%] | Eff P2dB [%] | Eff P3dB [%] |
|------------|-----------|---------------|----------|----------|----------|------------|-----------------|--------------|--------------|--------------|
| 902        | 22.36     | 548.35        | 784.81   | 855.45   | 904.28   | 70.55      | 903.93          | 68.81        | 70.06        | 70.55        |
| 915        | 22.76     | 554.38        | 781.56   | 850.54   | 896.90   | 71.12      | 898.50          | 69.64        | 70.80        | 71.12        |
| 928        | 23.07     | 554.35        | 766.80   | 831.53   | 874.67   | 71.28      | 856.45          | 70.13        | 71.14        | 71.22        |

**8. User Guide**

**8.1 Biasing**



*Figure 3 –Application board pin configuration*

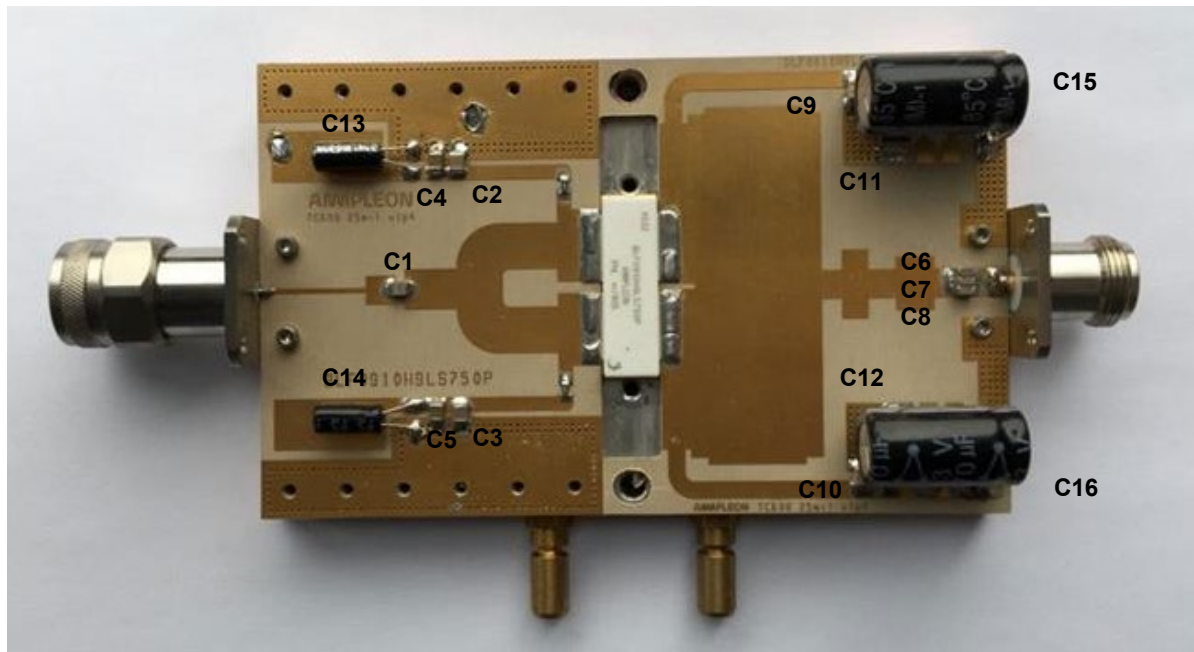
*Table 5 – Pin description*

| Symbol            | Pin | Description  |
|-------------------|-----|--|
| RF <sub>IN</sub>  | 1   | RF input   |
| RF <sub>OUT</sub> | 2   | RF output  |
| V <sub>GS</sub>   | 3,4 | Gate-source voltage (connect to either pin 3 or 4)               |
| V <sub>DS</sub>   | 5,6 | Drain-source voltage   |
| GND               | 7   | Negative supply terminal for V <sub>DS</sub> and V <sub>GS</sub> |

**8.2 Bill of Materials**

*Table 6 – Bill of Materials*

| Part                    | Description                       | Value           | Remark                |
|-------------------------|-----------------------------------|-----------------|-----------------------|
| C1, C2, C3, C6, C7, C8, | Multilayer ceramic chip capacitor | 560 pF          | ATC800B               |
| C4, C5                  | Multilayer ceramic chip capacitor | 1uF / 50V       | GRM32RR71H105KA01L    |
| C9, C10                 | Multilayer ceramic chip capacitor | 47 pF           | ATC100B               |
| C11, C12                | Multilayer ceramic chip capacitor | 4.7uF / 100V    | TDK C5750X7R2A475KT/A |
| C13, C14                | Electrolytic capacitor            | 10uF / 63V      |                       |
| C15, C16                | Electrolytic capacitor            | 470uF / 63V     |                       |
| R1, R2                  | Chip resistor                     | 10 Ω            | R0806                 |
| R3, R4                  | Chip resistor                     | 3.3 Ω           | BOURNS CRS2512        |
| R5                      | Shunt resistor                    | 0.01Ω           | Ohmite\FC4L110R010FER |
| T1                      | LD MOS transistor                 | BLF0910H9LS750P | Ampleon               |
| Input PCB               | TC600                             |                 | 25 mil thickness      |
| Output PCB              | TC600                             |                 | 25 mil thickness      |



*Figure 4 –Application board components placement*

### 8.3 Temperature behavior

For operation of this demo board water or air cooling should be applied.  
Water cooling temperature should be kept below 60 degC.

### 8.4 Device markings

*Table 7 – Module specifics*

| Parameter    | Value              |
|--------------|--------------------|
| Manufacturer | Ampleon            |
| Device       | BLF0910H9LS750P    |
| Comments     | Engineering sample |

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