This application note provides a general mounting recommendation/guideline suitable for plastic over-molded packages.
Mounting and soldering of RF transistors in over-molded plastic packages

Revision history

<table>
<thead>
<tr>
<th>Rev</th>
<th>Date</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>AN11183#2</td>
<td>20160302</td>
<td>Modifications</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• The format of this document has been redesigned to comply with the new identity guidelines of Ampleon.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Legal texts have been adapted to the new company name where appropriate.</td>
</tr>
<tr>
<td>AN11183#1</td>
<td>20121106</td>
<td>Initial version.</td>
</tr>
</tbody>
</table>

Contact information

For more information, please visit: http://www.ampleon.com

For sales office addresses, please visit: http://www.ampleon.com/sales
1. Introduction

1.1 General (mounting recommendations RF power)

This document is intended to guide customers in ways to solder RF Power transistors in Over-Molded Plastic (OMP) packages used as drivers (low-medium power) and final amplifiers (high-power). Each customer has an own way of designing applications and mounting the devices, so therefore it is not possible to cover all specific requirements. The intention of this document is to provide a general mounting recommendation/guideline suitable for plastic over-molded packages.

1.2 Definition

The following words in this document:
“Heat sink” refers to the application heat sink located under the PCB.
“Exposed heat spreader” refers to the exposed metal underneath the plastic over molded devices (or Cu base).
"Footprint or solder land“ is used to define the area on which to solder.

1.3 Main product groups

The introduction of LDMOS transistors started with the use of an air cavity package. The construction consists of a metal flange, on to which is brazed an insulated ring-frame with leads. The crystals (LDMOS) with input and output capacitors are eutectic soldered onto the flange. Gold wire bonds (later aluminum) are used to make the connection between the lead and the crystal. As a final step, the package is closed with a lid; see illustration in Figure 1.

Some customers prefer the air cavity packages to be soldered in their application, meaning no thermal compound/paste under the flange. A key reason to follow this route is improved thermal conductivity, resulting in an improved mean time to failure (MTTF). OMP packages came on the roadmap later. With the arrival of OMP packages, came the request for straight as well as gull wing (surface mount) leaded packages; see illustration in Figure 2. Outlines of some OMP packages are presented in Figure 3 and Figure 4.
Fig 2. Standard OMP package design; top and bottom view
Fig 3.  SOT1223-1 package outline drawing; straight lead outline
Mounting and soldering of RF transistors in over-molded plastic packages

HSOP4: plastic, heatsink small outline package; 4 leads

SOT1224-1

Fig 4. SOT1224-1 package outline drawing; gull wing outline

Note
1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

Dimensions (mm are the original dimensions)

| Unit | A   | A1  | A2  | A3  | A4  | b   | c   | D(1) | D1  | D2  | E(1) | E1  | E2  | e   | H_E | L_p | Q   | v   | w   | y   | θ   |
|------|-----|-----|-----|-----|-----|-----|-----|------|-----|-----|------|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| mm   | 3.9 | 0.2 | 3.65| 0.06| 3.90| 0.27| 20.62| 19.00| 16.05| 10.01| 8.18 | 5.89 | 13.5 | 1.10| 2.07| 7°  |
| nom  | 0.1 | 3.60| 0.35| 0   | 3.85| 0.22| 20.57| 18.95| 16.00| 9.96 | 8.13 | 5.85 | 13.2 | 0.95| 2.02| 2°  |
| min  | 0   | 3.55| -0.02| 0 | 3.80| 0.17| 20.52| 18.90| 15.95| 9.91 | 8.08 | 5.79 | 12.9 | 0.80| 1.97| 2°  |

Note
1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

References

<table>
<thead>
<tr>
<th>Outline version</th>
<th>IEC</th>
<th>JEDEC</th>
<th>JEITA</th>
</tr>
</thead>
<tbody>
<tr>
<td>SOT1224-1</td>
<td>IEC</td>
<td>JEDEC</td>
<td>JEITA</td>
</tr>
</tbody>
</table>

Issue date

12-04-25

© Ampleon Netherlands B.V. 2016. All rights reserved.

Application note

Rev. 2 — 2 March 2016

6 of 40
2. Substrate designs

2.1 Types of substrates

Depending on the power management and device layout (straight leads or gull wing), there are a number of mounting options:

- PCB with vias (low to medium power driver device in gull wing); see Figure 25
- PCB bonded to a heat sink with a cavity (straight leads); see Figure 20
- PCB bonded to a heat sink with a pedestal (high-power device in gull wing); see Figure 25

2.2 PCB design

A footprint design describes the recommended dimensions of the solder lands on the PCB, to make reliable solder joints between the semiconductor package and the PCB.

OMP devices are presented in different formats including the lead size and pitch. For packages with small pitch, it is not possible to apply a solder resist bridge between two terminals. A Cu defined layout must be used in this case.

If a solder land is solder resist defined, the Cu must extend underneath the solder resist to allow for tolerances in Cu etching and solder resist placement during board production. Similarly, if a solder land is Cu defined, the solder resist must be away from the solder land to prevent bleeding of the solder resist onto the Cu pad. Two solder mask configurations are available, and are described in Section 2.2.1 “Solder Mask Defined Pads (SMDP)”

2.2.1 Solder Mask Defined Pads (SMDP)

2.2.1.1 Main leads (SMDP)

When the solder mask extends onto the solder lands, the remaining solderable area is termed Solder Mask Defined Pad (SMDP). The “effective” solder pad is equal to the copper area that is not covered by the solder mask as illustrated in Figure 5.
Using SMDP, the copper will normally extend 75 µm underneath the solder mask on all sides; in other words, the copper dimension is 0.15 mm larger than the solder mask dimension; see Figure 5. These values may vary depending on the class of PCBs used. This allows for tolerances in copper etching and solder mask placement during PCB production. It is possible to design a solder mask bridge in between the pads and the PCB aperture, also illustrated in Figure 5.

If a solder mask bridge is designed between the pads and the PCB aperture, the leads will lay on this bridge (see Figure 6).

![Fig 6. Lead resting on a SMDP](aaa-004711)

**2.2.1.2 Footprint dimensions (SMDP)**

Few package dimensions are required to define the footprint on the PCB. These are shown in Figure 7.

![Fig 7. Relevant package dimensions for footprint definition](aaa-004712)

**2.2.1.3 PCB Aperture dimensions (SMDP)**

The package body is placed through an aperture in the PCB, and onto the heat sink. The dimensions of the aperture in the PCB should be such that the package can be inserted through it. In general, apertures in a PCB are made with certain accuracy.

Therefore it is advisable to design the PCB aperture (Figure 8) larger than the maximum package body dimensions so there is always at least 200 µm left for package insertion.
Aperture dimension (AI and AW) =

\[ E_{\text{max}} \text{ (or } D_{\text{max}}) + 0.2 \text{ mm (allow insertion)} + \text{aperture accuracy fabrication (typically 0.2 mm)} \]

Due to different production methods, the corner radius of an aperture is at least 0.4 mm. For ease with package insertion through the PCB, it is advised that the minimum corner radius is used in PCB design. The copper and solder mask dimensions are summarized in Figure 9 and Figure 10.
Mounting and soldering of RF transistors in over-molded plastic packages

The main rules used to define the footprint dimensions are:

- The solder mask apertures are 250 µm larger than the package leads (the total dimensions are 500 µm larger). This accommodates that the placement accuracy of the package on the PCB is not critical.

- The copper extends 75 µm underneath the solder mask on all sides, that is the total dimensions are 150 µm larger than the copper dimensions.

- The solder mask must lay 150 µm away from the aperture on all sides. If a solder mask ridge is designed between the PCB aperture and the pads, it must be at least 100 µm wide.

The main results are summarized in Figure 11:

![Fig 11. Main rules in defining the SMDP footprint](image)

### 2.2.2 Non Solder Mask Defined Pads (NSMDP)

#### 2.2.2.1 Main leads (NSMDP)

If the solder mask layer starts outside of the solder lands, and does not cover the copper, it is referred to as Non Solder Mask Defined Pad (NSMDP). The “effective” solder pad is equal to the copper area as illustrated in Figure 12.

![Fig 12. Non Solder Mask Defined Pads (NSMDP)](image)
In case of NSMDP, the solder mask must be at least 75 µm away from the solder land on all sides. In other words, the solder mask dimension is 150 µm larger than the copper dimension. These values may vary depending on the class of PCBs used. The main requirement is that the solder mask does not extend onto the copper. This is shown in Figure 12. Basically, there is a large trench in the solder mask around the copper.

The package is placed through an aperture in the PCB. Note that the solder mask does not reach the edge of the PCB aperture: it must always be at least 150 µm away from the edge of the aperture.

If so desired, it is also possible to design a narrow bridge of solder mask between the pads and the aperture in the PCB (illustrated in Figure 12). This is not strictly necessary, as the PCB material is also non-solderable. Note that a solder mask bridge must have a minimum width of 100 µm.

A solder mask layer is approximately 20 µm thick, whereas the copper is 30 µm to 35 µm thick. Thus, the solder mask is lower than the copper, and the lead will rest on the copper; see Figure 13.

2.2.2.2 Footprint dimensions (NSMDP)

Few package dimensions are required to define the footprint on the PCB. These are shown in Figure 7.

2.2.2.3 PCB Aperture dimensions (NSMDP)

The package body is placed through an aperture in the PCB, and onto the heat sink. The dimensions of the aperture in the PCB should be such that the package can be inserted through it. In general, apertures in a PCB are made with certain accuracy. A typical PCB cut-out for the aperture is at least 200 µm larger than the maximum package body dimensions; see Figure 8. The aperture dimensions (Al and Aw) for NSMDP are identical to the SMDP aperture dimensions.

The copper and solder mask dimensions for the packages are summarized for the NSMD situation in Figure 14 and Figure 15. Note: the 45 degrees drain lead angle (used for some outlines) is considered as negligible and therefore not taken into account in the solder mask/footprint designs.
The main rules used to define the copper footprint dimensions are:

- The copper pads are 250 µm larger than the package leads, on the three outer sides (the total dimensions are 500 µm larger). This value is relatively large, so that placement accuracy of the package on the PCB is not critical.

- The distance between the two copper pads is equal to the aperture dimension, plus 325 µm per side, to accommodate 100 µm of solder mask if desired. In other words, the copper lies 325 µm away from the aperture.

The main rules used to define the solder mask dimensions are:

- The solder mask must lay 150 µm away from the aperture.
- Must be at least 100 µm wide.
- And it must also lay 75 µm away from the copper. The solder mask lays 75 µm outside the copper on all sides, i.e. the total dimensions are 150 µm larger than the copper dimensions.

The main results are summarized in Figure 16:
The package outline and PCB footprints of Ampleon plastic packages can be found by clicking "Packages" in the "Looking for products" panel on the product information page of the Ampleon website at http://www.ampleon.com. The unique identifier for the PCB footprint is the Ampleon package outline code (the package SOT or SOD number, for example SOT834).

For general guidelines on board design, see Ref. 2 “IPC-7351” on page 36 Generic requirements for surface mount devices and land pattern standard.

The following paragraph explains how to read the PCB footprint. Figure 17 and Figure 18 show examples of a PCB footprint (with stencil and printed solder paste), as can be found on the Ampleon website.
Footprint information for reflow soldering of HSOP16F package

Fig 17. SOT834-1 PCB footprint; straight leads

Dimensions in mm

<table>
<thead>
<tr>
<th>Dimension</th>
<th>Value</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>sp</td>
<td>-0.025 mm</td>
<td>around copper</td>
</tr>
<tr>
<td>sr</td>
<td>+0.075 mm</td>
<td>around copper</td>
</tr>
<tr>
<td>1.45</td>
<td>(4 x)</td>
<td></td>
</tr>
<tr>
<td>0.60</td>
<td>(10 x)</td>
<td></td>
</tr>
<tr>
<td>11.78</td>
<td>(2 x)</td>
<td></td>
</tr>
<tr>
<td>11.50</td>
<td></td>
<td></td>
</tr>
<tr>
<td>12.00</td>
<td></td>
<td></td>
</tr>
<tr>
<td>17.10</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Fig 18. SOT822-1 PCB footprint; gull wing
The soldering process is carried out under a set of process parameters that include accuracies in the process, and semiconductor package, board, and stencil tolerances.

The footprint design is directly related to these aspects of the soldering process; the calculation of these dimensions is based on process parameters that are compliant with modern machines and a state-of-the-art process.

The substrates used for mounting the packages can be made of various materials with different properties. Due to the increased transistor density in the latest semiconductor technologies, and higher current (power) handling requirements, generation of heat has become a major limitation of the semiconductor performance. By applying an exposed pad or heat sink in the semiconductor package, in combination with thermal vias in the PCB, the heat can be transferred from the active die to the outside world. Four examples of capped vias are shown in Figure 19. Note that the only difference lies in the solder resist pattern.

3. Substrate design rules

The heat sink design depends primarily on dissipated heat and on the other components located on the PCB. These vary from one application to the next. Therefore there are no general recommendations on the size and thickness of the heat sink. In this section, a guide is provided on issues to consider during substrate design for gull wing and straight lead OMP packages.

3.1 Substrate design – straight lead devices

A typical substrate design is shown in Figure 20. The size of the cavity in the heat sink is defined by the package. For easy placement of the package into the heat sink cavity, the cavity width and length must be greater than the width and length of the package. Ampleon recommends making both the width and the length of the heat sink cavity 100 \( \mu \text{m} \) larger than the maximum package dimensions E and D shown in Figure 3 “SOT1223-1 package outline drawing; straight lead outline”.

Cavity dimension = \( E \) (or \( D \)) + 0.1 mm + tolerance.
For the PCB, the aperture should be larger (+ 0.2 mm) than the cavity in the heat sink. This is because of the risk of positional inaccuracy of the aperture in the PCB and the ensuing risk of placing the package leads on the ridge of solder mask. This risk does not exist with the heat sink cavity. As the tolerance in the heat sink cavity varies per application, the end values are not given in this document.

It is essential that after mounting these packages, the package leads make good contact with the PCB pads, and that the exposed heat spreader makes good contact with the heat sink. The main parameters are listed as follows:

- PCB thickness (Pt); see Figure 21
- Thickness of the interface (adhesive) between the PCB and the heat sink
- Solder thickness under the lead (Sl)
- Depth of the heat sink cavity or height
- Thickness of solder between the exposed heat spreader and the heat sink (Sf)
- Standoff height (Q): this is the distance between the exposed heat spreader and the bottom of the leads and is defined by the package; see Figure 21.

All of these parameters will vary due to their tolerances. Determining the cavity depth is a simple calculation of a worst case tolerance stack up; however it can end up in a value too large for normal production (the leads are likely to lay too high above the PCB). A common approach is to use the square root of sum of the square method.

Two main factors must be taken into account with the design of the heat sink cavity depth:

- When the cavity is too deep, the leads are lifted during soldering; see Figure 22. Consequently, the heat spreader is not soldered onto the heat sink. With a PCB edge close to the package, this could lead to high stresses.
• When the cavity is shallow, the distance between the solder of the leads and the exposed heat spreader becomes shorter, increasing the chance of solder bridging resulting to short circuits; see Figure 23.

**Fig 23. Cavity design too shallow**

In Figure 24, a sample substrate with cavity is illustrated.

**Fig 24. Sample substrate with cavity for soldering straight leads components**

### 3.2 Substrate design – gull wing devices

One of the main differences between straight and gull wing packages is the nature of the leads: gull wing packages are more compatible with surface mounting. The exposed heat spreader and the leads are almost on the same plane for gull wing devices. This requires the exposed heat sink on the substrate to be almost at the same plane as the PCB. The use of substrates with heat sinks or vias filled PCB depends on the thermal management (that is high or low-power device). Typical configurations are illustrated in Figure 25.

**Fig 25. Substrate design configurations; gull wing device**
Issues to consider include:

- Coplanarity of leads
- Distance between the bottom of lead to exposed heat spreader (A4 in Figure 4, also called stand-off height)
- Solder thickness (paste and perform)
- Distance between pedestal height and top of PCB

Figure 26 shows a sample substrate design with pedestal for soldering gull wing devices.

4. Solder paste printing

Solder paste printing (Figure 27) provides a consistent and controlled amount of solder paste on to the substrate. It requires a stencil aperture to be completely filled with paste. When the board is released from the stencil, the solder paste is supposed to adhere to the board so that all of the paste is released from the stencil aperture and a good solder paste deposit remains on the board. Ideally, the volume of solder paste on the board should equal the ‘volume’ of the stencil aperture. In practice, however, not all of the solder paste is released from the stencil aperture. The percentage of paste released depends largely on the aperture dimensions, that is, the length and width and the depth (the stencil thickness). If a stencil aperture becomes very small, the paste will no longer release completely. Furthermore, stencil apertures must be larger if a thicker stencil is used.

Another important factor is the aperture shape, that is, whether the aperture is rectangular, trapezoidal, or otherwise. Paste release also depends - among others – on the loading and speed of the squeegee, the board separation speed, the printing direction and the aperture orientation. In essence, all of these parameters must be adjusted so that all solder paste deposits on one board, from the smallest to the largest, are printed properly.
A second important aspect in solder paste printing is smearing. If some solder paste bleeds between the stencil and the board during one printing stroke, then the next board may not fit tightly to the stencil, allowing more paste to bleed onto the bottom of the stencil. As a result, the solder paste may eventually form bridges that stretch from one paste deposit to the next. If a bridge is narrow enough, it will snap open during reflow as the volume of molten solder seeks to attain minimum surface area. A wider bridge, however, may remain stable, resulting in a short-circuit.

Consequences of insufficient solder paste printing are usually open contacts or bad joints. These may arise because:

- the solder paste deposit is not sufficiently high: components or their leads may not make proper contact with the paste, resulting in open circuits or bad joints, or
- there is insufficient solder volume for a proper solder joint, also resulting in open circuits, or
- the activator is used up rapidly in a small solder paste deposit, so that the paste no longer properly wets the component metallization, also resulting in open circuits.

### 4.1 Stencil design – thickness and aperture size

To achieve a difference in printed solder paste volumes, it is possible to use a stencil that has a different thickness at different locations. An example of this is the step-stencil. This, however, is only recommended if there is no other solution.

Stencils are commonly made from Nickel; they may be either electro-formed or laser-cut. Stencils are illustrated in Figure 28 and typical stencil thickness is given in Table 1.
AN11183
Mounting and soldering of RF transistors in over-molded plastic packages

In most cases, the OMP package will be mounted on a PCB after the rest of the substrate has been populated. A typical process flow includes:

- Solder paste printing
- Solder preform placement (where required)
- Component placement (including the OMP package)
- Reflow
- Inspection

The height of the solder on the PCB pads will depend on the stencil that was used for printing.

Another parameter in the stencil design is the aperture size. As a general rule, the stencil apertures must be 25 μm smaller than the solder lands, on all sides. In other words, the solder paste lays 25 μm inward from the solder land edge. This usually results in stencil aperture dimensions that are 50 μm smaller than the corresponding solder land dimensions; see Figure 29.

Table 1. Stencil thickness

<table>
<thead>
<tr>
<th>Semiconductor package pitch</th>
<th>Stencil thickness</th>
</tr>
</thead>
<tbody>
<tr>
<td>≥ 0.5 mm</td>
<td>150 μm</td>
</tr>
<tr>
<td>0.4 mm to 0.5 mm</td>
<td>100 μm to 125 μm</td>
</tr>
</tbody>
</table>

In most cases, the OMP package will be mounted on a PCB after the rest of the substrate has been populated. A typical process flow includes:

- Solder paste printing
- Solder preform placement (where required)
- Component placement (including the OMP package)
- Reflow
- Inspection

The height of the solder on the PCB pads will depend on the stencil that was used for printing.

Another parameter in the stencil design is the aperture size. As a general rule, the stencil apertures must be 25 μm smaller than the solder lands, on all sides. In other words, the solder paste lays 25 μm inward from the solder land edge. This usually results in stencil aperture dimensions that are 50 μm smaller than the corresponding solder land dimensions; see Figure 29.
Another exception lies with the very large solder lands, such as when printing solder paste on a heat sink land. In that case, it is advised to print an array of smaller solder paste deposits. The solder paste should cover approximately 20 % of the total land area. It is also advised to keep the solder paste away from the edges of this land: the solder paste pattern, including the spacing between the deposits, should have coverage of 35 % of the land area; see Figure 30 and Figure 31.

A paste-printing pattern for exposed die pads is illustrated by the example shown in Figure 32. An HVQFN48 with an exposed pad of 5.1 mm x 5.1 mm, for example, should have nine solder paste deposits that are arranged in a three-by-three array. The solder paste deposits are 0.76 mm x 0.76 mm, with 0.37 mm spacing in between.

This way, the solder paste area is 9 (deposits) x (0.76 mm x 0.76 mm), and dividing this by the land area 5.1 mm x 5.1 mm yields a solder paste coverage of approximately 20 % of the total land area. Similarly, the solder paste pattern (the paste, plus the area between the deposits) has a length of 3.02 mm. The pattern area, 3.02 mm x 3.02 mm, divided by the land area, yields a solder past pattern coverage of approximately 35 % of the land area.
Samples of soldered devices are illustrated in Figure 33.
No-clean flux solder paste and no-clean solder wire should be used, so the PCB and the package do not have to be cleaned after reflow or manual soldering.

The footprint design describes the recommended solder land on the PCB to make a reliable solder joint between the semiconductor package and the PCB. A proven solder material is SnPb, but due to legislation, the industry has changed to Pb-free solutions such as Sn/Ag/Cu (SAC). These require higher temperature than SnPb solders. Process requirements for solder paste printing and reflow soldering, for SnPb and Pb-free, are also discussed in this document.
Printed-circuit boards and footprints are not only used as mechanical carriers for electronic components; they also provide the electronic interconnection between these components and also between these components and the outside world. These electronic components may be semiconductors, or other types such as capacitors and resistors. Through component selection and the use of Cu interconnections between the components, an electronic system, such as a mobile phone, can be assembled on a PCB.

Common board finishes include NiAu, Organic Solderability Preservative (OSP), and immersion Sn. Although finishes may look different after reflow, and some appear to have better wetting characteristics than others, all common finishes can be used, provided that they are in accordance with the specifications.

Examples of other issues in board quality are:

1. Tolerances on the pad and solder resist dimensions and component placement
2. Maximum board dimensions
3. Flatness

The application board is usually a mix of large and small components together with thermal design features. In board designs where large components or thermal design features are in close proximity to small components, solderability issues may arise (that is, hotspots).

5. Solder paste and preform

Solder paste and preforms are used during soldering. Table 2 provides a summary of the possible combinations. The “X” marked cells are typically used in the industry.

<table>
<thead>
<tr>
<th>Lead shape and solder type</th>
<th>Gull wing</th>
<th>Straight leads</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Leads</td>
<td>Heat spreader</td>
</tr>
<tr>
<td>Solder paste</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>Solder preform</td>
<td>-</td>
<td>X</td>
</tr>
</tbody>
</table>

5.1 Solders

In line with European legislation, it is recommended to use a Pb-free solder paste or preform, although exemptions are granted for selected applications such as automotive.

A wide variety of Pb-free solder pastes are available, containing combinations of tin, copper, antimony, silver, bismuth, indium and other elements. The different types of Pb-free solder pastes/preforms have a wide range of melting temperatures.
As a substitute for SnPb solder, the most common Pb-free paste/preforms used is SAC, which is a combination of tin (Sn), silver (Ag) and copper (Cu). These three elements are usually in the range of 3 % to 4 % of Ag and 0 % to 1 % of Cu, which is near eutectic. SAC typically has a melting temperature of approximately 217 °C, and it requires a reflow temperature of more than 235 °C (Table 3).

Care should be taken when selecting a solder, and note that solder types are categorized by solder sphere size. For small packages or fine pitch applications, solder paste type 3 or better (Type 4 or 5) is recommended.

A no-clean solder paste or preform does not require cleaning after reflow soldering and is therefore preferred, if this is possible within the process window.

Preforms with pre-applied flux are available in the market. When additional flux is applied on the preform (that is, manually, such as with a brush, pen or dipping), extra care must be taken. Excessive flux increases the chance of voids in the solder joint. For more information on the solder paste and solder preforms, contact your solder supplier.

6. Reflow soldering procedure

Ampleon advises to use a convection oven rather than a conduction or radiation oven. A convection oven provides a uniform heat and a very controlled temperature (± 2°C). Moreover, it allows soldering a wide range of products due to the temperature uniformity. During the reflow soldering process all parts of the board are subjected to an accurate temperature/time profile.

A temperature profile essentially consists of three phases:

- **Pre-heat**: the board is warmed up to a temperature that lies lower than the melting point of the solder alloy.

- **Reflow**: the board is heated to a peak temperature well above the melting point of the solder, but below the temperature at which the components and boards are damaged.

- **Cooling down**: the board is cooled down, so that soldered joints freeze before the board exits the oven.

The peak temperature during reflow has an upper and a lower limit.

6.1 Lower limit of peak temperature

The minimum peak temperature must at least be high enough for the solder to make reliable solder joints. This is determined by solder paste characteristics; contact your paste supplier for details.
6.2 Upper limit of peak temperature

The maximum peak temperature must be lower than the temperature at which the components are damaged. This is defined by Moisture Sensitivity Level (MSL) testing of the package. The maximum body temperature during reflow soldering depends on the body size and on the demand to respect the package MSL.

6.3 The temperature at which the boards are damaged

This is a board characteristic; contact your board supplier for details.

When a board is exposed to the reflow profile, certain areas on the board become hotter than others: a board has hotspots (the hottest areas) and cold spots (the coldest areas). Cold spots are usually found in sections of the board that hold a high density of large components, as these soak up much heat, or near heat sinks. Hotspots, on the other hand, are found in areas with few components, or only the smallest components, and with little Cu nearby. Finally, the board dimensions, and the board orientation in the oven, can also affect the location of hot and cold spots.

The hot spot on a board may not surpass the upper limit to the peak temperature. Similarly, the cold spot must reach the lower limit at least. Thus, it is imperative that all areas on the board, including the hot and cold spots, fall within the upper and lower limits of the peak temperature.

![Figure 34. Temperature profiles for large and small components](image-url)

In Figure 34, the largest and smallest component go through cold and hot spots of the reflow profile. In the pre-heat phase, the hot spots heat up rapidly to a temperature lower than the melting point of the solder alloy. They may remain at this temperature for a while. Note however, that small solder paste deposits should not remain at an intermediate temperature for so long that their activator runs out: for small solder paste deposits, a fast temperature profile is preferred. The cold spots on the board warm up far more slowly. The oven settings should be planned so that the cold as well as the hot spots reach roughly the same temperature by the end of the pre-heat phase.
The second phase in the reflow profile is the reflow zone, in which the solder melts and forms soldered joints. The minimum peak temperature, in which all solder joints in the cold as well as the hot spots must reach, depends on the solder alloy. However, no region on the board may surpass a maximum peak temperature, as this would result in component and/or board damage. Even if the cold and hot spots start the reflow phase with roughly the same temperature, the hot spots will reach a higher peak temperature than the cold spots. Yet, both the hot spots and the cold spots must lie within the allowed peak temperature range. This may require some adjustment of the oven temperature settings and conveyor belt speeds. In extreme cases, even the board layout may have to be optimized to limit the temperature difference between the cold and the hot spots.

When reflow soldering, the peak temperature should never exceed the temperature at which either the components or the board are damaged. For reflow soldering with SnPb solder, the peak temperature should be greater than 215 °C. When soldering with SAC, the peak temperature should be greater than 235 °C. Note that this usually implies a smaller process window for Pb-free soldering, thus requiring tighter process control.

The curves in Figure 35 represent the actual temperature profiles for a number of different spots on a board. The bottom line represents the cold spot, and the top line corresponds to the hot spot. The minimum and maximum allowed peak temperatures are indicated. At the top left, some regions on the board are exposed to temperatures that are too high, resulting in damage. At the bottom left, some regions on the board are exposed to temperatures that are too low, resulting in unreliable joints. At the right, all of the regions on the board have peak temperatures that fall within the upper and lower limits.

Proper joint formation should always be verified by visual inspection through a microscope. In general, Pb-free solder is a little less successful at wetting than SnPb solders; SAC fillets have a larger contact angle between the fillet and the wetted surface. More information is given concerning wetting behavior in Section 7 “Inspection”.

Fig 35. Fitting both the hot and cold spots into the required peak temperature range
6.4 An example of a reflow profile used for internal study

The reflow soldering profile should be calibrated with a thermocouple glued down on the device to prevent a temperature offset. All reflow activities were performed in a belt oven with an inert atmosphere (N2). During calibration, the zone temperature and belt speed are varied and the device temperature monitored and compared to the JEDEC recommendations; see Table 4.

Table 4. SAC Reflow profile classification (JEDEC JSTD020d)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Unit</th>
<th>Specification</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>Time above liquidus</td>
<td>seconds</td>
<td>60 to 150</td>
<td>SAC Liquidus is 217 °C</td>
</tr>
<tr>
<td>Ramp-up slope (max)</td>
<td>°C / s</td>
<td>3</td>
<td>Heating-up rate</td>
</tr>
<tr>
<td>Max. package temperature</td>
<td>°C</td>
<td>245 to 260</td>
<td>Package size dependent</td>
</tr>
<tr>
<td>Liquidus temperature</td>
<td>°C</td>
<td>217</td>
<td>Melting point</td>
</tr>
<tr>
<td>Time to peak temperature</td>
<td>minutes</td>
<td>8 (max)</td>
<td>-</td>
</tr>
<tr>
<td>Average ramp-down rate</td>
<td>°C / s</td>
<td>6 (max)</td>
<td>Cooling down rate</td>
</tr>
</tbody>
</table>

SAC (Pb-free) solder used was with a melting point of 217 °C, and a peak soldering temperature of 235 °C to 245 °C (JEDEC JSTD020d). A sample reflow profile is shown in Figure 36.

Fig 36. Sample reflow profile - SAC solder

7. Inspection

7.1 Wetting appearance

Notice the difference between SnPb and Pb-free solder. In Figure 37a (SnPb), the solder lands have been wetted completely. Meanwhile in Figure 37b, the solder has left part of the solder lands non-wetted.
Another visual aspect with Pb-free soldering is that Pb-free solder joints (Figure 38b) tend to be less shiny than SnPb solder joints (Figure 38a), and may show striation marks. This is due to the different microstructure formed during solidification. Although SnPb solder joints should be rejected if they appear as shown in Figure 38b, this is normal appearance for Pb-free solder joints and no reason for rejection.

Non-wetting of lead frame parts as a result of punching or sawing is not a reason for rejection. Other inspection methods besides optical inspection, such as for design and process development purposes are:

- Automatic optical inspection (AOI)
- Examination by x-ray
- Cross-sectional analysis
- Dye penetration test
- CSAM (scanning acoustic microscope), MIL-STD-883E

8. Reworking

An incorrectly soldered package lead can be repaired by heating it with the tip of a soldering iron. In this case, it is sufficient to heat the lead until the solder melts completely,
and a new device should not be necessary. In other situations, however, there may be a need to replace the package. The rework process should then consist of the following steps:

- Removal of old package
- Site preparation
- New package placement
- Soldering new package

### 8.1 Package removal

Prior to removal of the old package it is advised to dry-bake the PCB for 4 hours at 125 °C.

If the package is going to be submitted for failure analysis, use a soldering iron that is ESD-safe. It is essential that both leads are heated simultaneously, while a vacuum wand nozzle ([Figure 39](#)) is attached to the top of the package body for lifting it off.

The process steps are as follows:

- Set the hotplate (localized heating) to a temperature high enough to melt the solder. This value depends on the type of solder used to attach the package.
- Place module on the hot plate with heat localized to the device.
- Attach a vacuum wand nozzle (at temperature) to the top of the package body.
- Watch carefully as the solder joint melts.
• As soon as the solder melts, lift the package off the PCB using the vacuum wand. Do not lift the package before the solder in the joints has melted completely, as this may damage the package and the PCB.

Throughout this process, care must be taken that there is no contact with neighboring components.

8.2 Site preparation

After the package has been removed, the PCB pads must be prepared for the new package. Prepare the pads by removing any excess solder and/or flux remains. Ideally this is done on an appropriate de-soldering station. Alternately, use a soldering iron set to the temperature specified for the solder that was originally used to attach the package. Clean the pads using the soldering iron and solder wick, or another in-house technique. Note: use a temperature high enough to just liquefy the solder but not damage the PCB.

After most of the solder has been removed from a solder land, a very thin layer of solder will be left, on top of a few intermetallic layers. In the case of Cu pads, for example, there will be layers of Cu3Sn, Cu6Sn5, and finally solder, on top of the Cu. The top layer of solder is easily solderable; see Figure 40.

If, however, the pad is heated too much during removal of the rejected IC package, and during site preparation, the top two layers will also be converted into Cu3Sn. In this situation, there will only be the Cu3Sn inter-metallic layer on top of the Cu. Unfortunately, Cu3Sn is not solderable (poor solderability). Therefore, care must be taken during reject package removal and site redress, that the solder lands are heated only as much as is absolutely necessary.

8.3 Placement of the new package

If the heat sink was discarded, mount a new heat sink. Next, mount a new package in much the same way as the original package was mounted. Reuse of removed packages is not recommended. Finally, the new package is soldered to the PCB in the same manner as the original package.
9. Appendices

9.1 Appendix I: Moisture Sensitivity Level (MSL)

If moisture is trapped inside an OMP surface mount package, and the package is exposed to a reflow temperature profile, the moisture may turn into steam, which expands rapidly. This may damage the inside of the package (delamination), and could result in a cracked semiconductor package body (the popcorn effect). A package’s sensitivity to moisture, or Moisture Sensitivity Level (MSL), depends on the package characteristics and on the temperature it is exposed to during reflow soldering. The MSL of semiconductor packages can be determined through standardized tests in which the packages are moisturized to a predetermined level and then exposed to a temperature profile. Studies have shown that small and thin packages reach higher temperatures during reflow than larger packages. Therefore, small and thin packages must be classified at higher reflow temperatures. The temperatures that packages are exposed to are always measured at the top of the package body. Depending on the damage after this test, an MSL of 1 (not sensitive to moisture) to 6 (very sensitive to moisture) is attached to the semiconductor package. For every plastic over-molded product, this MSL is given on a packing label on the shipping box. Each package is rated at two temperatures, for SnPb and Pb-free soldering conditions. An example of a packing label is given in Figure 41.

Note the two MSLs circled in red corresponding to the two reflow processes.

Fig 41. Example of MSL information on packing label

MSL corresponds to a certain out-of-bag time (or floor life). If semiconductor packages are removed from their sealed dry-bags and not soldered within their out-of-bag time, they must be baked prior to reflow, in order to remove any moisture that might have soaked into the package. MSLs and temperatures on the packing labels are to be respected at all times. Naturally, this also means that semiconductor packages with a critical MSL may not remain on the placement machine between assembly runs. Nor should partial assembled boards, between two reflow steps, be stored longer than indicated by the MSL level. The semiconductor package floor life, as a function of the MSL, can be found in Table 5.
9.2 Appendix II: ESD

Damage to semiconductors from Electro Static Discharge (ESD) is a major cause of rejection and poses an increased risk to miniaturized packages. Electrostatic charge can be stored in many things, for example, man-made fiber clothing, moving machinery, objects with air blowing across them, plastic storage bins, sheets of paper stored in plastic envelopes, paper from electrostatic copying machines and people. Electrostatic discharge is the transfer of an electrostatic charge between bodies at different potentials and occurs with direct contact or when induced by an electrostatic field. It is recommended that the following ESD precautions be complied with.

9.2.1 Workstations for handling ESD sensitive components

Figure 42 shows a working area suitable for safely handling electrostatic-sensitive devices. The following precautions should be observed.

- Workbench and floor surface should be lined with anti-static material.
- Persons at a workbench should be earthed via a wrist strap and a resistor.
- All mains-powered equipment should be connected to the mains via an earth leakage switch.
- Equipment cases should be grounded.
- Relative humidity should be maintained between 40 % and 50 %.
- An ionizer should be used to neutralize objects with immobile static charges in case other solutions fail.
- Keep static materials, such as plastic envelopes and plastic trays away from the workbench. If there are any such static materials on the workbench remove them before handling the semiconductor devices.
- Refer to the current version of the handbook EN 100015 (CECC 00015) “Protection of Electrostatic Sensitive Devices”, which explains in more detail how to arrange an ESD protective area for handling ESD sensitive devices.

### Table 5. MSL levels (J-STD-020D)

<table>
<thead>
<tr>
<th>MSL [1]</th>
<th>Floor life</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Time</td>
</tr>
<tr>
<td>1</td>
<td>Unlimited</td>
</tr>
<tr>
<td>2</td>
<td>1 year</td>
</tr>
<tr>
<td>3a</td>
<td>4 weeks</td>
</tr>
<tr>
<td>3</td>
<td>168 hours</td>
</tr>
<tr>
<td>4</td>
<td>72 hours</td>
</tr>
<tr>
<td>5</td>
<td>48 hours</td>
</tr>
<tr>
<td>5a</td>
<td>24 hours</td>
</tr>
<tr>
<td>6</td>
<td>6 hours</td>
</tr>
</tbody>
</table>

[1] MSL 6 packages must be baked before use, after which they have a 6-hour floor life.

Table 5. MSL levels (J-STD-020D)
9.2.2 Receipt and storage of components

Packing for electrostatic devices should be made of anti-static/conductive materials. Warning labels on both primary and secondary packing show that the contents are sensitive to electrostatic discharge. The electronic components should be kept in their original packing whilst in storage. If a bulk container is partially unpacked, the unpacking should be done at a protected workstation. Any electronic components that are stored temporarily should be re-packed in conductive or anti-static packing or carriers.

9.2.3 PCB assembly

All tools used during assembly, including soldering tools and solder baths, must be grounded. All hand tools should be of conductive or anti-static material and where possible should not be insulated. Standard precautions for manual handling of electrostatic-sensitive devices need to be taken into account.
10. Abbreviations

<table>
<thead>
<tr>
<th>Acronym</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>LDMOS</td>
<td>Laterally Diffused Metal-Oxide Semiconductor</td>
</tr>
<tr>
<td>MSL</td>
<td>Moisture Sensitivity Level</td>
</tr>
<tr>
<td>MTTF</td>
<td>Mean Time To Failure</td>
</tr>
<tr>
<td>NSMDP</td>
<td>Non Solder Mask Defined Pads</td>
</tr>
<tr>
<td>OMP</td>
<td>Over-Molded Plastic</td>
</tr>
<tr>
<td>PCB</td>
<td>Printed Circuit Board</td>
</tr>
<tr>
<td>RF</td>
<td>Radio Frequency</td>
</tr>
<tr>
<td>RH</td>
<td>Relative Humidity</td>
</tr>
<tr>
<td>SAC</td>
<td>Sn (Tin) Ag (Silver) Cu (Copper)</td>
</tr>
<tr>
<td>SMDP</td>
<td>Solder Mask Defined Pads</td>
</tr>
<tr>
<td>SnPb</td>
<td>Sn (Tin) Pb (Lead)</td>
</tr>
</tbody>
</table>

11. References

[1] IPC/JEDEC J-STD-020D  

[2] IPC-7351  
Generic requirements for Surface Mount Design and Land Pattern Standard, IPC

[3] EN 100015/CECC 00015  
Protection of Electrostatic Sensitive Devices, European Standard

[4] 3997.750.04888  
Quality reference handbook, Ampleon

Acceptability of Electronic Assemblies, IPC

Test Method Standards for Microcircuits
12. Legal information

12.1 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. Ampleon does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

12.2 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, Ampleon does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. Ampleon takes no responsibility for the content in this document if provided by an information source outside of Ampleon.

In no event shall Ampleon be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or work or work charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, Ampleon’ aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of Ampleon.

Right to make changes — Ampleon reserves the right to change to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — Ampleon products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an Ampleon product can reasonably be expected to result in personal injury, death or severe property or environmental damage. Ampleon and its suppliers accept no liability for inclusion and/or use of Ampleon products in such equipment or applications and therefore such inclusion and/or use is at the customer’s own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. Ampleon makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using Ampleon products, and Ampleon accepts no liability for any assistance with applications or customer product design. It is customer’s sole responsibility to determine whether the Ampleon product is suitable and fit for the customer’s applications and products planned, as well as for the planned application and use of customer’s third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

Ampleon does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer’s applications or products, or the application or use by customer’s third party customer(s). Customer is responsible for doing all necessary testing for the customer’s applications and products using Ampleon products in order to avoid a default of the applications and the products or of the application or use by customer’s third party customer(s). Ampleon does not accept any liability in this respect.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Evaluation products — This product is provided on an “as is” and “with all faults” basis for evaluation purposes only. Ampleon, its affiliates and their suppliers expressly disclaim all warranties, whether express, implied or statutory, including but not limited to the implied warranties of non-infringement, merchantability and fitness for a particular purpose. The entire risk as to the quality, or arising out of the use or performance, of this product remains with customer.

In no event shall Ampleon, its affiliates or their suppliers be liable to customer for any special, indirect, consequential, punitive or incidental damages (including without limitation damages for loss of business, business interruption, loss of use, loss of data or information, and the like) arising out the use of or inability to use the product, whether or not based on tort (including negligence), strict liability, breach of contract, breach of warranty or any other theory, even if advised of the possibility of such damages. Notwithstanding any damages that customer might incur for any reason whatsoever (including without limitation, all damages referenced above and all direct or general damages), the entire liability of Ampleon, its affiliates and their suppliers and customer’s exclusive remedy for all of the foregoing shall be limited to actual damages incurred by customer based on reasonable reliance up to the greater of the amount actually paid by customer for the product or five dollars (US$5.00). The foregoing limitations, exclusions and disclaimers shall apply to the maximum extent permitted by applicable law, even if any remedy fails of its essential purpose.

12.3 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

Any reference or use of any 'NXP' trademark in this document or in or on the surface of Ampleon products does not result in any claim, liability or entitlement vis-à-vis the owner of this trademark. Ampleon is no longer part of the NXP group of companies and any reference to or use of the 'NXP' trademarks will be replaced by reference to or use of Ampleon’s own trademarks.
13. Tables

Table 1. Stencil thickness ......................... 21
Table 2. Overview of application areas for solder pastes and preforms ....................... 25
Table 3. Minimum peak temperature for soldering per alloy (JEDEC JSTD020d) ............. 26
Table 4. SAC Reflow profile classification (JEDEC JSTD020d) .................................. 29
Table 5. MSL levels (J-STD-020D) ................ 34
Table 6. Abbreviations ............................. 36
14. Figures

Fig 1. Over-molded versus air cavity package ............ 3
Fig 2. Standard OMP package designs; top and bottom view ............................................. 4
Fig 3. SOT1223-1 package outline drawing; straight lead outline ........................................... 5
Fig 4. SOT1224-1 package outline drawing; gull wing outline .............................................. 6
Fig 5. Solder Mask Defined Pads (SMDP) with solder mask bridge ........................................ 7
Fig 6. Lead resting on an SMDP ............................... 8
Fig 7. Relevant package dimensions for footprint definition ....................................................... 8
Fig 8. PCB aperture dimensions ............................. 9
Fig 9. Cu footprint dimensions for SMDP ................. 9
Fig 10. Solder mask dimensions for SMDP ............... 9
Fig 11. Main rules in defining the SMDP footprint ...... 10
Fig 12. Non Solder Mask Defined Pads (NSMDP) ......10
Fig 13. Lead resting on an NSMDP ......................... 11
Fig 14. Cu footprint dimensions for NSMDP ............ 12
Fig 15. Solder mask dimensions for NSMDP .......... 12
Fig 16. Main rules in defining the NSMDP ................13
Fig 17. SOT834-1 PCB footprint; straight leads ......14
Fig 18. SOT822-1 PCB footprint; gull wing .............15
Fig 19. Capped vias; from left to right: via tenting from top, via tenting from bottom, via capping from bottom, via encroached from bottom ...... 16
Fig 20. Substrate design configuration with cavity for straight lead devices ...............................16
Fig 21. Main rules in defining substrates cavity ..........17
Fig 22. Cavity design too deep .............................17
Fig 23. Cavity design too shallow .........................18
Fig 24. Sample substrate with cavity for soldering straight leads components ............................18
Fig 25. Substrate design configurations; gull wing device .......................................................18
Fig 26. Example of substrate design for soldering gull wing component ....................................19
Fig 27. Stencil printing ........................................20
Fig 28. Manual stencils .......................................21
Fig 29. Solder paste printing on NSMDP and SMDP ....22
Fig 30. Paste coverage ........................................22
Fig 31. Pattern coverage .....................................22
Fig 32. Solder paste dimensions on the land area for an exposed die pad ..................................23
Fig 33. Examples of soldered gull wing and straight leads devices ......................................... 24
Fig 34. Fig 34. Temperature profiles for large and small components .......................................27
Fig 35. Fitting both the hot and cold spots into the required peak temperature range ................28
Fig 36. Sample reflow profile – SAC solder ............ 29
Fig 37. Difference in wetting appearance between SnPb and Pb-free solder joints .....................30
Fig 38. Difference in visual appearance between SnPb (shiny) and Pb-free (dull) solder joints ......30
Fig 39. Vacuum wand nozzle .................................31
Fig 40. Overheating and Cu3Sn intermetallic formation .32
Fig 41. Example of MSL information on packing label .33
Fig 42. ESD protected workstation environment .......35