Power LDMOS transistor Rev. 2 — 7 November 2019

Product profile 1.

1.1 General description

550 W LDMOS packaged asymmetric Doherty power transistor for base station applications at frequencies from 2100 MHz to 2200 MHz.

Typical performance Table 1.

Typical RF performance at T_{case} = 25 °C in an asymmetrical Doherty demo circuit. V_{DS} = 29/32 V; I_{Dq} = 900 mA (main); $V_{GS(amp)peak}$ = 1.2 V, unless otherwise specified.

Test signal	f	V _{DS}	P _{L(AV)}	G p	ησ	ACPR
	(MHz)	(V)	(W)	(dB)	(%)	(dBc)
1-carrier W-CDMA	2110 to 2170	29	90	15.9	50.5	–28.5 <mark>[1]</mark>
	2110 to 2170	32	115	16.3	49.8	–29.1 <mark>[1]</mark>

[1] Test signal: 1-carrier W-CDMA; 3GPP test model 1; 64 DPCH; PAR = 9.9 dB at 0.01 % probability on CCDF.

1.2 Features and benefits

- Excellent ruggedness
- High efficiency
- Low thermal resistance providing excellent thermal stability
- Lower output capacitance for improved performance in Doherty applications
- Designed for low memory effects providing excellent digital pre-distortion capability
- Internally matched for ease of use
- Integrated ESD protection
- For RoHS compliance see the product details on the Ampleon website

1.3 Applications

RF power amplifiers for base stations and multi carrier applications in the 2100 MHz to 2200 MHz frequency range

2. Pinning information

Table 2. P	inning		
Pin	Description	Simplified outline	Graphic symbol
1	drain2 (peak)		0.7
2	drain1 (main)		2,7
3	gate1 (main)	5	
4	gate2 (peak)		3
5	source [1]		
6	video decoupling (peak)		"F]
7	video decoupling (main)		1, 6 <i>aaa-014884</i>

[1] Connected to flange.

3. Ordering information

Table 3.	Ordering information
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Type number	Package				
	Name	Description	Version		
BLC10G22XS-551AVT	-	air cavity plastic earless flanged package; 6 leads	SOT1258-4		

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{DS}	drain-source voltage		-	65	V
V _{GS(amp)main}	main amplifier gate-source voltage		-6	+9	V
V _{GS(amp)peak}	peak amplifier gate-source voltage		-6	+9	V
T _{stg}	storage temperature		-65	+150	°C
Tj	junction temperature	<u>[1]</u>	-	225	°C
T _{case}	case temperature	operating [1]	-40	+125	°C

[1] Continuous use at maximum temperature will affect the reliability, for details refer to the online MTF calculator.

5. Thermal characteristics

Table 5.Thermal characteristics

Symbol	Parameter	Conditions	Тур	Unit
R _{th(j-c)}	thermal resistance from junction to case	V _{DS} = 32 V; I _{Dq} = 900 mA (main); V _{GS(amp)peak} = 1.024 V; T _{case} = 80 °C		
		P _L = 87 W	0.24	k/W
		P _L = 110 W	0.22	k/W

6. Characteristics

Table 6. DC characteristics	stics
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 $T_j = 25 \ ^{\circ}C$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Main dev	vice					
V _{(BR)DSS}	drain-source breakdown voltage	V _{GS} = 0 V; I _D = 1.8 mA	65	-	-	V
V _{GS(th)}	gate-source threshold voltage	V _{DS} = 10 V; I _D = 180 mA	1.6	2.0	2.4	V
V _{GSq}	gate-source quiescent voltage	V _{DS} = 32 V; I _D = 800 mA	-	2.2	-	V
I _{DSS}	drain leakage current	V _{GS} = 0 V; V _{DS} = 32 V	-	-	2.8	μA
I _{DSX}	$_{\rm X}$ drain cut-off current $$V_{\rm GS}$ = V_{\rm GS(th)}$ + 2.37 V; $V_{\rm DS}$ = 10 V$$		-	34	-	A
I _{GSS}	gate leakage current	V _{GS} = 9 V; V _{DS} = 0 V	-	-	280	nA
g _{fs}	forward transconductance	V _{DS} = 10 V; I _D = 9.0 A	-	20.5	-	S
R _{DS(on)}	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 2.37 V;$ I _D = 6.3 A	-	72	108	mΩ
Peak dev	vice		1	1	1	
V _{(BR)DSS}	drain-source breakdown voltage	V _{GS} = 0 V; I _D = 3.8 mA	65	-	-	V
V _{GS(th)}	gate-source threshold voltage	V _{DS} = 10 V; I _D = 380 mA	1.6	2.0	2.4	V
V _{GSq}	gate-source quiescent voltage	V _{DS} = 32 V; I _D = 1900 mA	-	2.2	-	V
I _{DSS}	drain leakage current	V _{GS} = 0 V; V _{DS} = 32 V	-	-	2.8	μA
		$V_{GS} = V_{GS(th)} + 2.37 V;$ $V_{DS} = 10 V$	-	57	-	A
I _{GSS}	gate leakage current	V _{GS} = 9 V; V _{DS} = 0 V	-	-	280	nA
9 _{fs}	forward transconductance	V _{DS} = 10 V; I _D = 19.0 A	-	39.0	-	S
R _{DS(on)}	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 2.37 V;$ I _D = 13.3 A	-	37	62	mΩ

Table 7.RF characteristics

Test signal: 1-carrier W-CDMA; PAR = 9.6 dB at 0.01 % probability on the CCDF; 3GPP test model 1; 1 to 64 DPCH; f_1 = 2112.5 MHz; f_2 = 2167.5 MHz; RF performance at V_{DS} = 32 V; I_{Dq} = 1000 mA (main); $V_{GS(amp)peak}$ = 1.2 V; T_{case} = 25 °C; unless otherwise specified; in an asymmetrical Doherty production test circuit at frequencies from 2110 MHz to 2170 MHz.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
G _p	power gain	P _{L(AV)} = 115 W	15.0	16.0	-	dB
RL _{in}	input return loss	P _{L(AV)} = 115 W	-	-15	-10	dB
η _D	drain efficiency	P _{L(AV)} = 115 W	46	50	-	%
ACPR	adjacent channel power ratio	P _{L(AV)} = 115 W	-	-29	-24	dBc

Table 8. RF characteristics

Test signal: 1-carrier W-CDMA; PAR = 9.6 dB at 0.01 % probability on the CCDF; 3GPP test model 1; 1 to 64 DPCH; f = 2167.5 MHz; RF performance at V_{DS} = 32 V; I_{Dq} = 1000 mA (main); $V_{GS(amp)peak}$ = 1.2 V; T_{case} = 25 °C; unless otherwise specified; in an asymmetrical Doherty production test circuit at a frequency of 2170 MHz

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
PARO	output peak-to-average ratio	P _{L(AV)} = 145 W	6.0	6.5	-	dB
P _{L(M)}	peak output power	P _{L(AV)} = 145 W	566	650	-	W

7. Test information

7.1 Ruggedness in Doherty operation

The BLC10G22XS-551AVT is capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 32 V; I_{Dq} = 1000 mA; $V_{GS(amp)peak}$ = 1.15 V; f = 2110 MHz; P_L = 235 W (5 dB OBO); 1-carrier W-CDMA; 3GPP test model 1; 64 DPCH; PAR = 9.6 dB at 0.01 % probability on CCDF.

7.2 Impedance information

Table 9. Typical impedance of main device

Measured load-pull data of main device; $I_{Dq} = 900 \text{ mA}$ (main); $V_{DS} = 32 \text{ V}$; pulsed CW ($t_p = 100 \mu s$; $\delta = 10 \%$).

f	Z _S [1]	Z _L [1]	P _L [2]	η <mark>ρ ^[2]</mark>	G _p [2]			
(MHz)	(Ω)	(Ω)	(W)	(%)	(dB)			
Maximu	Maximum power load							
2110	2.8 – j6.5	1.6 – j4.0	298	58.2	15.2			
2140	3.3 – j7.0	1.8 – j3.5	298	60.2	15.8			
2170	4.1 – j7.2	1.6 – j3.5	295	57.6	15.6			
Maximu	m drain efficien	cy load						
2110	3.2 – j6.9	4.0 - j2.4	198	69.5	17.9			
2140	3.8 – j7.2	3.3 – j2.5	222	68.9	17.7			
2170	4.7 – j7.4	2.9 – j2.3	222	68.6	17.8			

[1] Z_S and Z_L defined in Figure 1.

[2] At 3 dB gain compression.

Table 10. Typical impedance of peak device

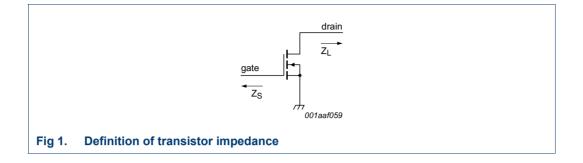
Measured load-pull data of peak device; I_{Dq} = 1900 mA (peak); V_{DS} = 32 V; pulsed CW (t_p = 100 μ s; δ = 10 %).

f	Z _S [1]	Z _L [1]	P _L [2]	η <mark>ρ <mark>[2]</mark></mark>	G _p [2]			
(MHz)	(Ω)	(Ω)	(W)	(%)	(dB)			
Maximu	Maximum power load							
2110	1.9 – j6.0	2.0 – j3.7	596	62.2	14.8			
2140	2.3 – j6.3	1.7 – j3.8	592	57.4	14.3			
2170	2.8 – j6.6	1.6 – j3.5	583	59.6	14.8			
Maximu	m drain efficiei	ncy load	·		"			
2110	2.0 – j6.0	2.7 – j2.8	502	67.4	15.9			
2140	2.5 – j6.3	2.9 – j2.7	468	66.4	16.0			
2170	3.0 – j6.7	2.3 – j2.5	471	66.6	16.2			

[1] Z_S and Z_L defined in Figure 1.

[2] At 3 dB gain compression.

Power LDMOS transistor



7.3 Test circuit

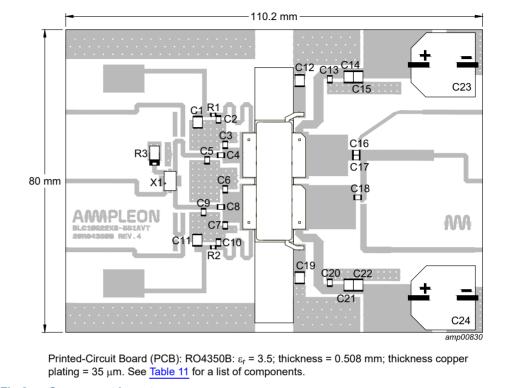


Fig 2. Component layout

Table 11. List of components

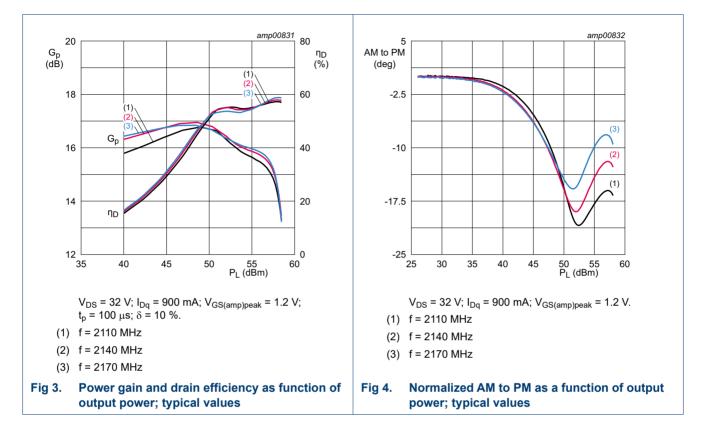
See Figure 2 for component layout.

Component	Description	Value	Remarks
C1, C11, C12, C14, C15, C19, C21, C22	multilayer ceramic chip capacitor	10 μF, 100 V	X7S
C2, C4, C8, C10, C13, C18, C20	multilayer ceramic chip capacitor	10 pF [1]	
C3	multilayer ceramic chip capacitor	0.5 pF [1]	
C5	multilayer ceramic chip capacitor	0.8 pF [1]	
C6, C7	multilayer ceramic chip capacitor	1.0 pF [1]	
C9	multilayer ceramic chip capacitor	0.8 pF [1]	
C16	multilayer ceramic chip capacitor	2.2 pF [1]	
C17	multilayer ceramic chip capacitor	2.7 pF [1]	
C23, C24	electrolytic capacitor	470 μF, 63 V	EEVFK1J471M
R1, R2	resistor	4.7 Ω	
R3	resistor	50 Ω, 25 W	Anaren: C16A50Z4
X1	hybrid coupler	2 dB, 90°	Anaren: Xinger III, X3C20F1-02

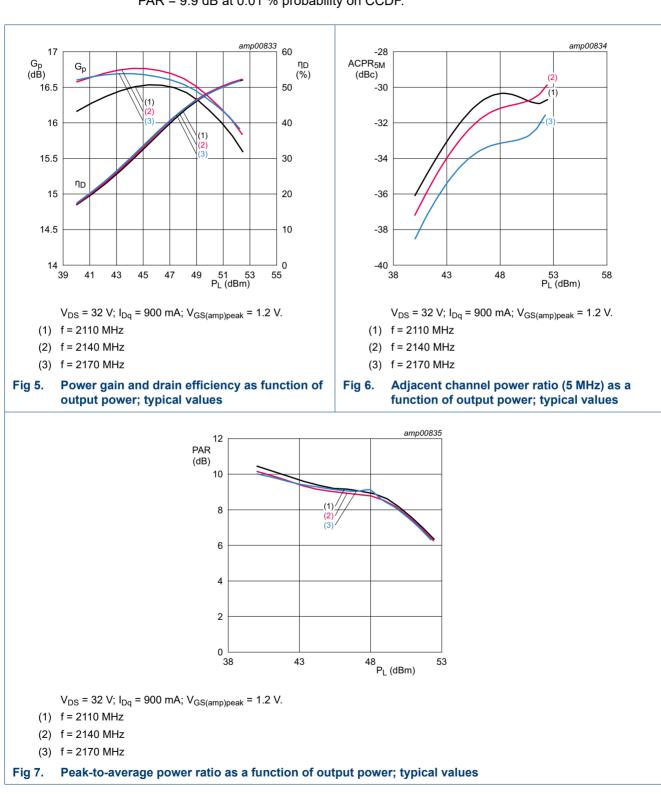
[1] Murata: GQM21 series.

7.4 Graphical data

7.4.1 Pulsed CW

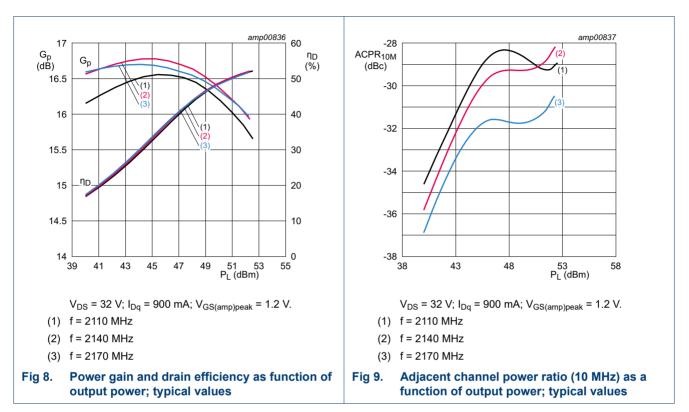


7.4.2 1-Carrier W-CDMA



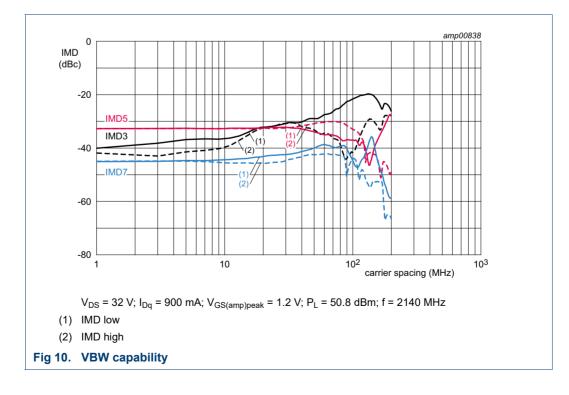
Test signal: 1-carrier W-CDMA; 3GPP test model 1; 1 to 64 DPCH (100 % clipping); PAR = 9.9 dB at 0.01 % probability on CCDF.

7.4.3 1-Carrier LTE



Test signal: 1-carrier LTE 10 MHz; PAR = 6.8 dB at 0.01 % probability on CCDF.

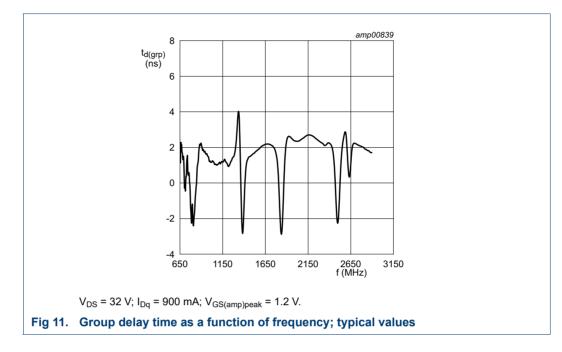
7.4.4 2-Tone VBW



BLC10G22XS-551AVT

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7.4.5 Group delay



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8. Package outline

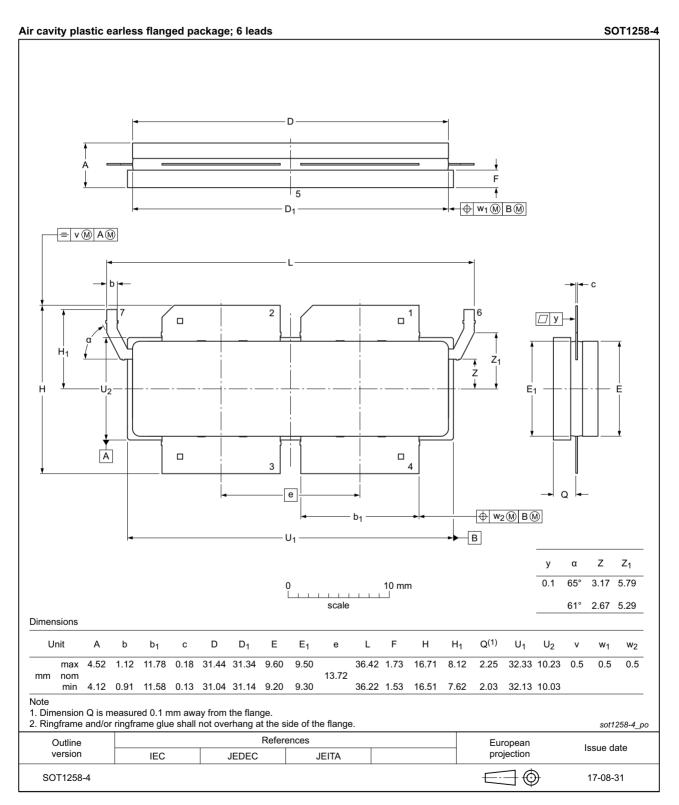


Fig 12. Package outline SOT1258-4

9. Handling information

CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the ANSI/ESD S20.20, IEC/ST 61340-5, JESD625-A or equivalent standards.

Table 12.ESD sensitivity

ESD model	Class
Charged Device Model (CDM); According to ANSI/ESDA/JEDEC standard JS-002	C3 🛄
Human Body Model (HBM); According to ANSI/ESDA/JEDEC standard JS-001	2 [2]

[1] CDM classification C3 is granted to any part that passes after exposure to an ESD pulse of 1000 V.

[2] HBM classification 2 is granted to any part that passes after exposure to an ESD pulse of 2000 V.

10. Abbreviations

Table 13. Abbreviations		
Acronym	Description	
3GPP	3rd Generation Partnership Project	
AM	Amplitude Modulation	
CCDF	Complementary Cumulative Distribution Function	
CW	Continuous Wave	
DPCH	Dedicated Physical CHannel	
ESD	ElectroStatic Discharge	
LDMOS	Laterally Diffused Metal-Oxide Semiconductor	
LTE	Long Term Evolution	
MTF	Median Time to Failure	
OBO	Output Back Off	
PAR	Peak-to-Average Ratio	
PM	Phase Modulation	
RoHS	Restriction of Hazardous Substances	
VBW	Video BandWidth	
VSWR	Voltage Standing Wave Ratio	
W-CDMA	Wideband Code Division Multiple Access	

11. Revision history

Table 14. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLC10G22XS-551AVT v.2	20191107	Product data sheet	-	BLC10G22XS-551AVT v.1
Modifications:	<u>Section 7.3 on page 6</u> : added section			
BLC10G22XS-551AVT v.1	20190307	Product data sheet	-	-

BLC10G22XS-551AVT

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Product data sheet

12. Legal information

12.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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