CLF24H4LS600PX

RF power GaN-SiC HEMT

AMPLEON

Rev. 0.14 — 23 October 2026 **Preliminary data sheet**

1. Product profile

1.1 General description

The CLF24H4LS600PX is a 600 W internally pre-matched and post-matched GaN HEMT power transistor optimized for best power and efficiency at frequencies from 2400 MHz to 2500 MHz.

The CLF24H4LS600PX is designed for high-power CW applications and is assembled in a high performance ceramic package.

Table 1. Application performance

RF performance at V_{DS} = 50 V; I_{Dq} = 20 mA; T_{amb} = 25 °C; soldered in demo board.

Test signal	f	$G_{p(max)}$	P_L [2]	η_D [2]
	(MHz)	(dB)	(W)	(%)
CW pulsed [1]	2400	18.3	735	76.3
	2450	18.7	694	75.8
	2500	19.0	635	74.9
CW	2400	17.9	719	75.5
	2450	18.3	679	74.9
	2500	18.6	622	73.8

[1] t_p = 100 µs; δ = 10 %

[2] At $P_{L(3dB)}$

1.2 Features and benefits

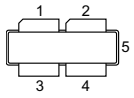
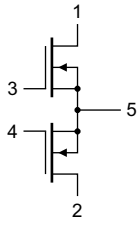
- High efficiency
- Excellent ruggedness under CW and CW pulsed conditions
- High output impedance
- Internally pre-matched and post-matched
- For RoHS compliance see the product details on the Ampleon website

1.3 Applications

- RF power amplifiers for applications in the 2400 MHz to 2500 MHz frequency range such as heating, plasma generator and other ISM applications

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	drain1		
2	drain2		
3	gate1		
4	gate2		
5	source [1]		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Package name	Orderable part number	12NC	Packing description	Min. orderable quantity (pieces)
SOT539B	CLF24H4LS600PXU	9349 610 95112	3BL-TRAY 60-fold; DP SOT539B_SIM	60

4. Limiting values

Table 4. Limiting values

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	source voltage	operating	-	55	V
V_{DS}	drain-source voltage		-	150	V
V_{GS}	gate-source voltage		−15	+2	V
I_{GF}	forward gate current	per section	-	31.2	mA
T_{stg}	storage temperature		−65	+150	°C
T_{ch}	active die channel temperature		-	225	°C

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(s-c)(IR)}$ [1]	thermal resistance from active die surface to case by Infrared measurement	V_{DS} = 50 V; P_{dis} = 300 W; T_{case} = 80 °C	0.22	K/W
$R_{th(ch-c)(FEA)}$	thermal resistance from active die channel to case by Finite Element Analysis	V_{DS} = 50 V; P_{dis} = 300 W; T_{case} = 80 °C	0.30	K/W

[1] Infrared (IR) thermal values are for reference only and cannot be used to determine performance or reliability.

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6. Characteristics

Table 6. DC characteristics

T_{amb} = 25 °C; per section unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 50 V; I_D = 62.4 mA	-	−2.8	-	V
V_{GSq}	gate-source quiescent voltage	V_{DS} = 50 V; I_D = 20 mA	-	−2.9	-	V
$I_{D(leak)}$	drain leakage current	V_{GS} = −10 V; V_{DS} = 50 V	-	-	15.1	mA
$I_{G(leak)}$	drain leakage current	V_{GS} = −10 V; V_{DS} = 50 V	-	-	15.1	mA
I_{GSS}	gate leakage current	V_{GS} = −8 V; V_{DS} = 0 V	-	-	3.02	mA
I_{DSX}	drain cut-off current	V_{DS} = 20 V; V_{GS} = 2 V	-	43	-	A

Table 7. RF characteristics

Clamped in production test circuit. Test signal: CW pulsed; t_p = 100 µs; δ = 10 %; f = 2450 MHz; RF performance at V_{DS} = 50 V; I_{Dq} = 20 mA; T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	P_L = 600 W	-	16.4	-	dB
RL_{in}	input return loss	P_L = 600 W	-	24.6	-	dB
η_D	drain efficiency	P_L = 600 W	-	72.1	-	%

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7. Test information

7.1 Ruggedness

The CLF24H4LS600PX is capable of withstanding a load mismatch corresponding to VSWR = 20 : 1 through all phases under the following conditions: V_{DS} = 50 V; I_{Dq} = 20 mA; P_L = 600 W; f = 2450 MHz; CW pulsed (t_p = 100 μs; δ = 10 %).

The CLF24H4LS600PX is capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 50 V; I_{Dq} = 20 mA; P_L = 600 W; f = 2450 MHz; CW.

7.2 Impedance information

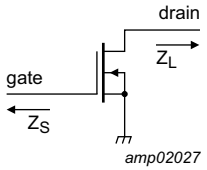


Fig 1. Definition of transistor impedance

Table 8. Typical impedance

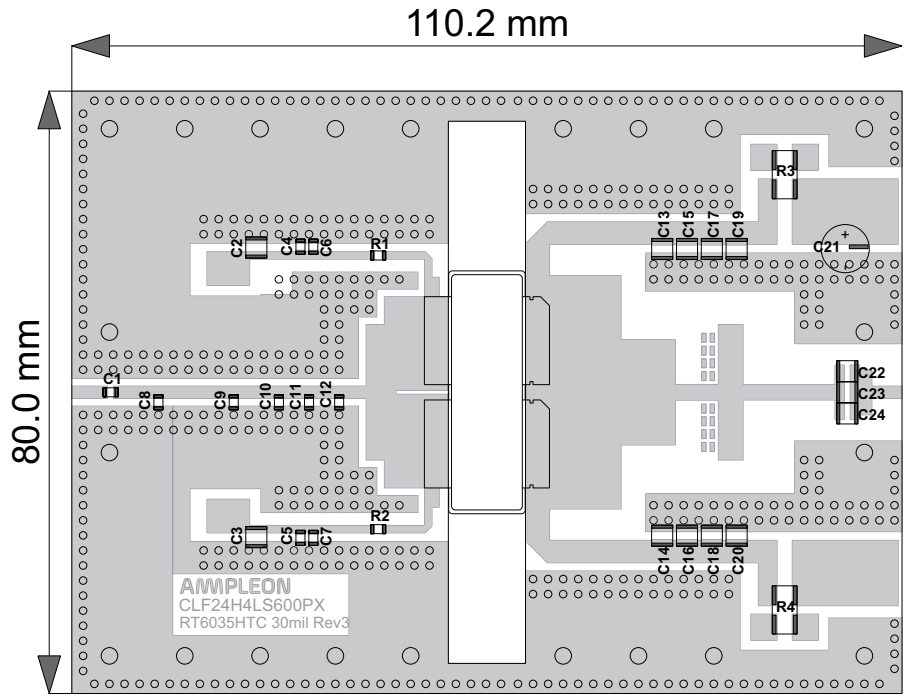
Measured Z_s and Z_L per section impedance; impedance info at V_{DS} = 50 V; I_{Dq} = 100 mA; P_L = 300 W.

f	Z_s	Z_L	$Z_{L(2H)}$ [1]
(MHz)	(Ω)	(Ω)	(Ω)
2400	1.79 – j6.87	1.96 – j1.31	0.56 + j0.14
2450	2.21 – j7.51	1.96 – j1.31	0.56 – j0.47
2500	2.80 – j8.10	1.53 – j1.48	0.59 – j1.31

[1] Optimum 2nd Harmonic impedances

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7.3 Test circuit



Printed-Circuit Board (PCB): Rogers RT6035HTC; ε_r = 3.6; thickness copper plating = 35 μm; See Table 9 for a list of components.

Fig 2. Component layout

Table 9. List of components

See Figure 2.

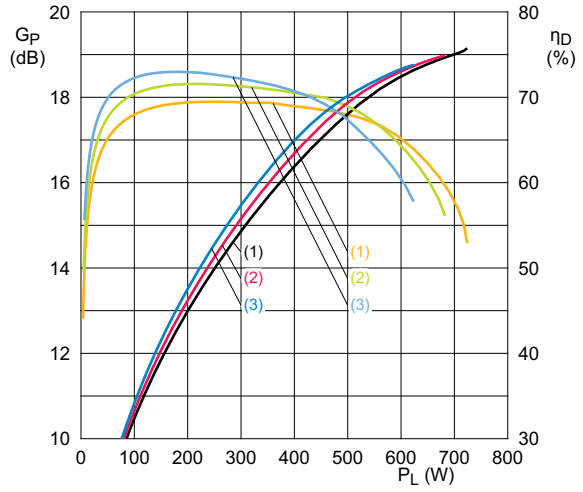
Component	Description	Value	Remarks
C1	multilayer ceramic chip capacitor	33 pF ± 5 %	[1]
C2, C3	multilayer ceramic chip capacitor	4.7 μF ± 10 %	SMD1206, X7R
C4, C5	multilayer ceramic chip capacitor	100 nF ± 10 %	SMD0805, X7R
C6, C7	multilayer ceramic chip capacitor	100 pF ± 5 %	[1]
C8	multilayer ceramic chip capacitor	0.4 pF	[1]
C9	multilayer ceramic chip capacitor	0.2 pF	[1]
C10	multilayer ceramic chip capacitor	0.7 pF	[1]
C11, C12	multilayer ceramic chip capacitor	0.8 pF	[1]
C13, C14, C15, C16	multilayer ceramic chip capacitor	1000 pF ± 5 %	ATC800B
C17, C18, C19, C20	multilayer ceramic chip capacitor	10 μF ± 10 %	TDK C3225X7R, 100 V
C21	electrolytic capacitor	220 μF ± 10 %	SMD, 63 V
C22, C23, C24	multilayer ceramic chip capacitor	12 pF ± 5 %	ATC800R120J500WT
R1, R2	resistor	22 Ω ± 5 %	SMD1206
R3, R4	resistor	10 mΩ ± 1 %	OHMITE

[1] American Technical Ceramics type 800A or capacitor of same quality.

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7.4 Graphical data

7.4.1 CW signal



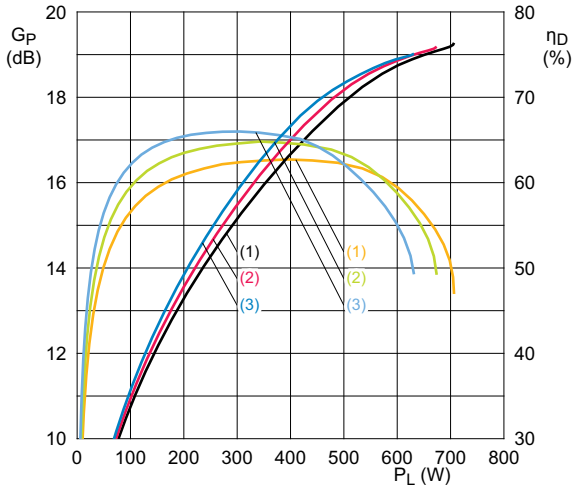
V_{DS} = 50 V; I_{Dq} = 20 mA.

(1) f = 2400 MHz

(2) f = 2450 MHz

(3) f = 2500 MHz

Fig 3. Power gain and drain efficiency as function of output power; typical values



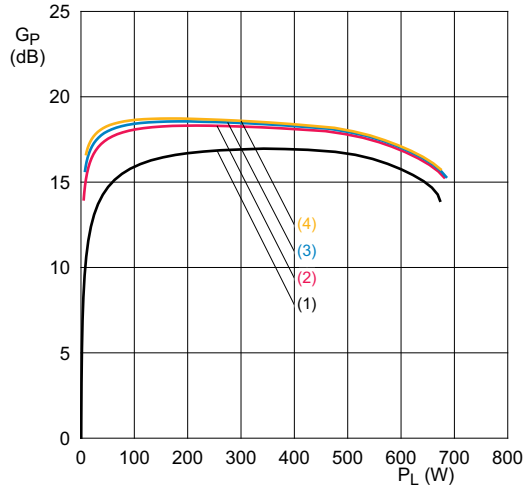
V_{DS} = 50 V; V_{gs} = −3.6 V.

(1) f = 2400 MHz

(2) f = 2450 MHz

(3) f = 2500 MHz

Fig 4. Power gain and drain efficiency as function of output power; typical values



V_{DS} = 50 V; f = 2450 MHz.

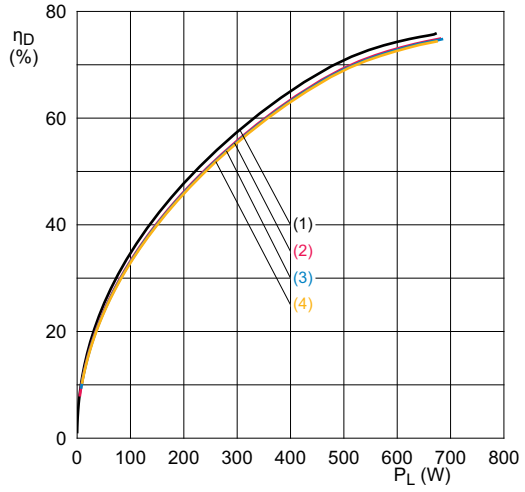
(1) V_{gs} = −3.6 V

(2) I_{Dq} = 20 mA

(3) I_{Dq} = 50 mA

(4) I_{Dq} = 100 mA

Fig 5. Power gain as a function of output power; typical values



V_{DS} = 50 V; f = 2450 MHz.

(1) V_{gs} = −3.6 V

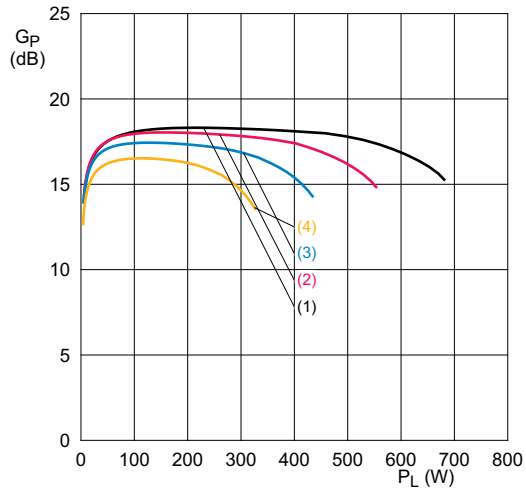
(2) I_{Dq} = 20 mA

(3) I_{Dq} = 50 mA

(4) I_{Dq} = 100 mA

Fig 6. Drain efficiency as a function of output power; typical values

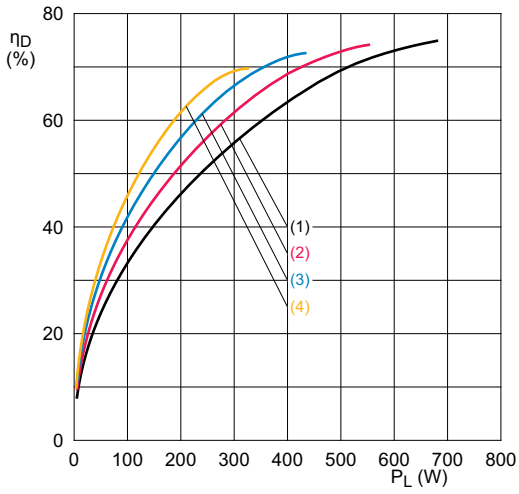
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I_{Dq} = 20 mA; f = 2450 MHz.

(1) V_{DS} = 50 V
(2) V_{DS} = 45 V
(3) V_{DS} = 40 V
(4) V_{DS} = 35 V

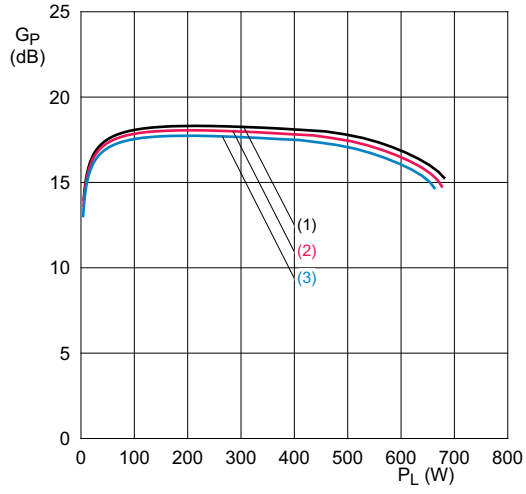
Fig 7. Power gain as a function of output power; typical values



I_{Dq} = 20 mA; f = 2450 MHz.

(1) V_{DS} = 50 V
(2) V_{DS} = 45 V
(3) V_{DS} = 40 V
(4) V_{DS} = 35 V

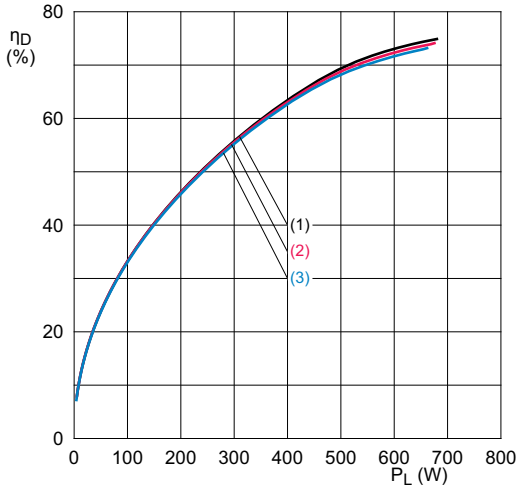
Fig 8. Drain efficiency as a function of output power; typical values



V_{DS} = 50 V; I_{Dq} = 20 mA; f = 2450 MHz.

(1) T_{amb} = 25 °C
(2) T_{amb} = 45 °C
(3) T_{amb} = 65 °C

Fig 9. Power gain as a function of output power; typical values

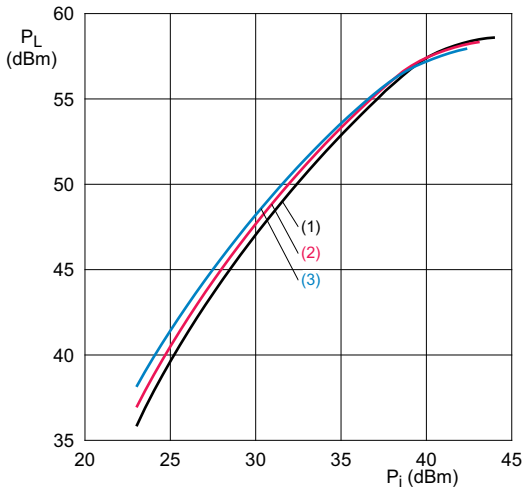


V_{DS} = 50 V; I_{Dq} = 20 mA; f = 2450 MHz.

(1) T_{amb} = 25 °C
(2) T_{amb} = 45 °C
(3) T_{amb} = 65 °C

Fig 10. Drain efficiency as a function of output power; typical values

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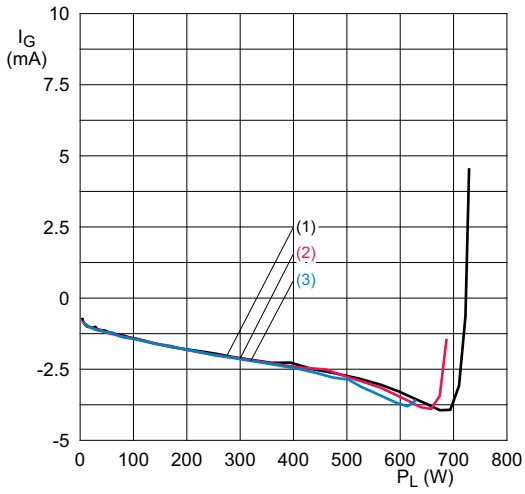
V_{DS} = 50 V; I_{Dq} = 20 mA.

(1) f = 2400 MHz

(2) f = 2450 MHz

(3) f = 2500 MHz

Fig 11. Output power as a function of input power; typical values



V_{DS} = 50 V; I_{Dq} = 20 mA.

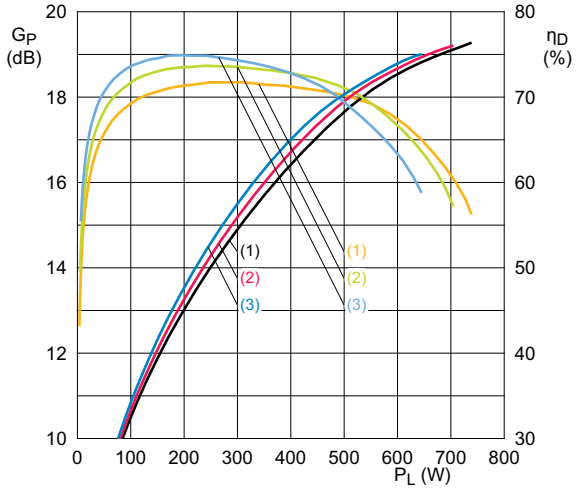
(1) f = 2400 MHz

(2) f = 2450 MHz

(3) f = 2500 MHz

Fig 12. Gate current as a function of output power; typical values

7.4.2 Pulsed signal



V_{DS} = 50 V; I_{Dq} = 20 mA; δ = 10 %; t_p = 100 µs.

(1) f = 2400 MHz

(2) f = 2450 MHz

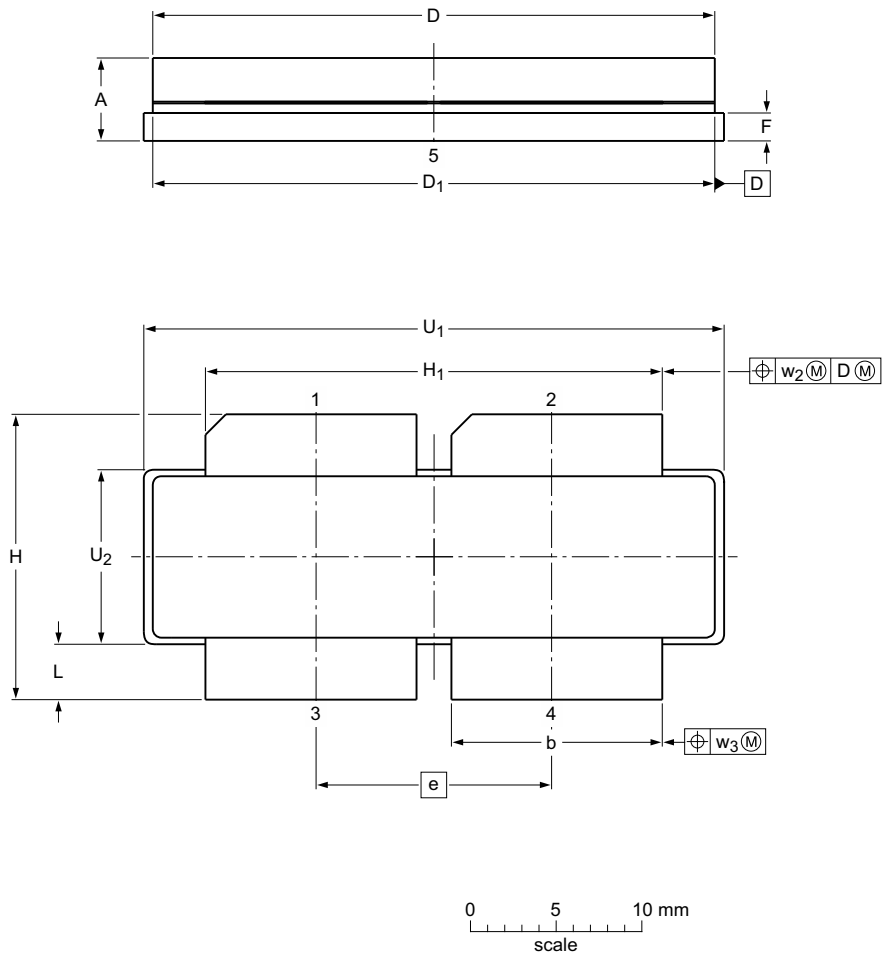
(3) f = 2500 MHz

Fig 13. Power gain and drain efficiency as function of output power; typical values

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8. Package outline

Earless flanged balanced ceramic package; 4 leads **SOT539B**



Dimensions

Unit[1]		A	b	c	D	D_1	E	E_1	e	F	H	H_1	L	Q	U_1	U_2	w_2	w_3
mm	max	4.7	11.81	0.18	31.55	31.52	9.5	9.53	13.72	1.75	17.12	25.53	3.48	2.26	32.39	10.29	0.25	0.25
	nom																	
	min	4.2	11.56	0.10	30.94	30.96	9.3	9.27		1.50	16.10	25.27	2.97	2.01	32.13	10.03		
inches	max	0.185	0.465	0.007	1.242	1.241	0.374	0.375	0.54	0.069	0.674	1.005	0.137	0.089	1.275	0.405	0.01	0.01
	nom																	
	min	0.165	0.455	0.004	1.218	1.219	0.366	0.365		0.059	0.634	0.995	0.117	0.079	1.265	0.395		

Note
1. millimeter dimensions are derived from the original inch dimensions.

sot539b_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT539B						~~12-05-02~~ 13-05-24

Fig 14. Package outline SOT539B

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9. Handling information

CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

Table 10. ESD sensitivity

ESD model	Class
Charged Device Model (CDM); According to ANSI/ESDA/JEDEC standard JS-002	C3 [1]
Human Body Model (HBM); According to ANSI/ESDA/JEDEC standard JS-001	1B [2]

[1] CDM classification C3 is granted to any part that passes after exposure to an ESD pulse of1000 V.

[2] HBM classification 1B is granted to any part that passes after exposure to an ESD pulse of 500 V.

10. Abbreviations

Table 11. Abbreviations

Acronym	Description
CW	Continuous Wave
GaN	Gallium Nitride
HEMT	High Electron Mobility Transistor
MTF	Median Time to Failure
RF	Radio Frequency
RoHS	Restriction of Hazardous Substances
SiC	Silicon Carbide
VSWR	Voltage Standing Wave Ratio

11. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
CLF24H4LS600PX v.0.14	<tbd>	Preliminary data sheet	-	-

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Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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