

AR201210

ART35FE, 81-108 MHz

v1.0 – September 29, 2020

AMPLEON

Application Report

Document information

Status v1.0

Abstract Measurement results of a demoboard design with the ART35FE in the 81-108 MHz bandwidth

1. Revision History

Table 1 – Report revisions

Revision	Date	Description	Author
1.0	2020.09.29	Initial document	

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5. General description

This report presents the measurement results of the demoboard designed for 81-108 MHz frequency band using the ART35FE transistor based on 65V ART technology. During assembly, the PCB has been screwed down without soldering it and the connection of the transistor has been made with a pressing block.

The dedicated demo-circuit is matched to 50 Ω at input and output.

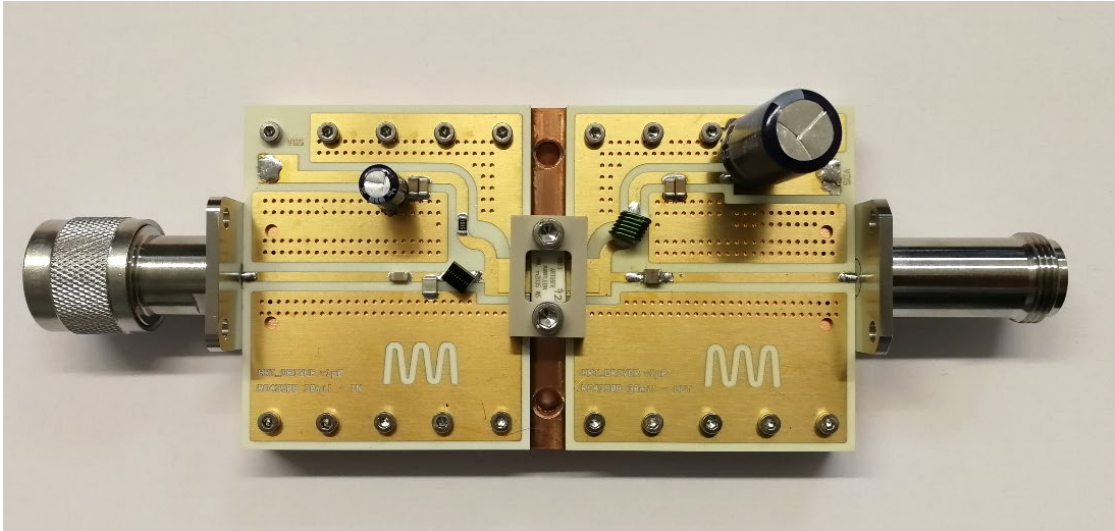


Figure 1 – Demo front view

Table 2 – Test circuit information

Parameter	Description	Unit
Laminate Type	Rogers 4350B	
Dk	3.48	
Df	0.0037 @10 GHz	
Laminate thickness	0.762	mm
Copper thickness	1 oz top/bottom	
Overall dimensions	106 x 60	mm
Cooling type	Indirect water cooling	
Device Package	SOT467	

6. Measured S-Parameters

Measurement conditions: $V_{DS}=65V$; $I_{DQ}=100mA$; $T_{cooling\ water}=25^{\circ}C$

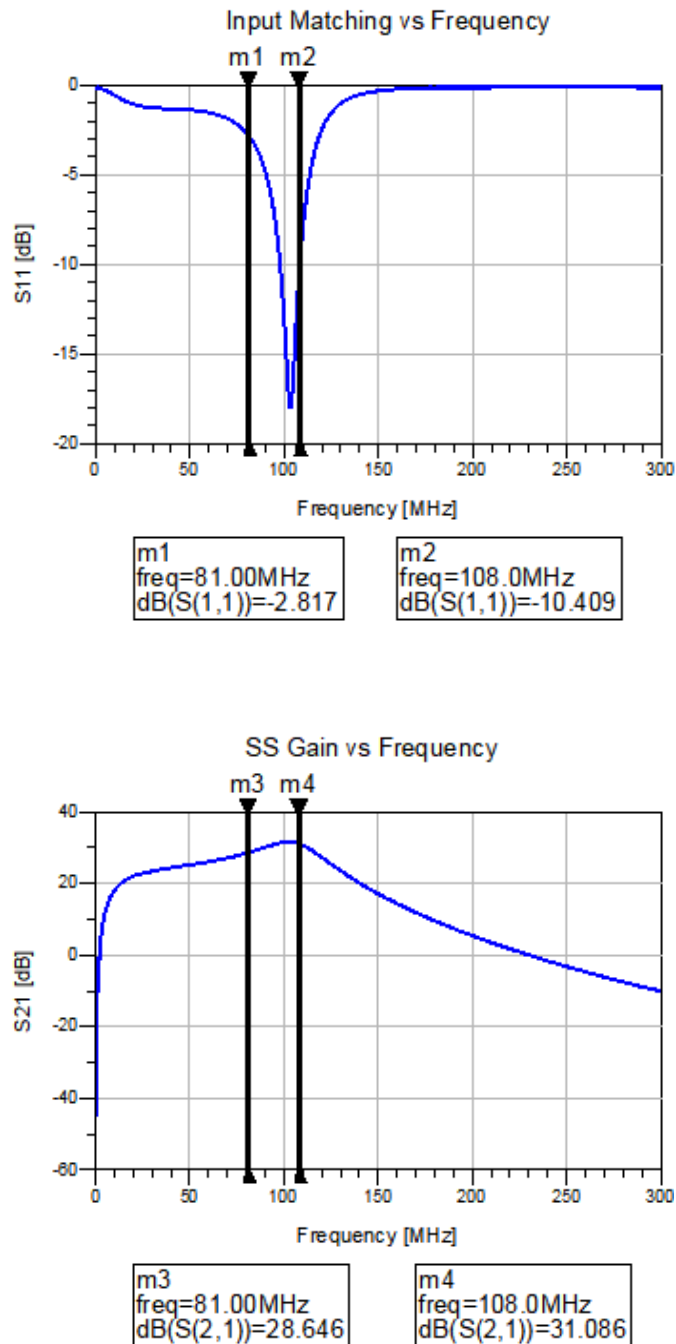


Figure 2 – Measured S parameters: Input Matching (top), Gain (bottom)

7. CW RF characteristics

Table 3 – Performance indication

Test signal: CW; RF performance at $V_{DS}=65V$; $I_{Dq}=10mA$; $T_{cooling\ water}=25^{\circ}C$

Symbol	Parameter	Conditions	Typical	Unit
f	Frequency		108	MHz
V_{DS}	Drain-source voltage		65	V
V_{GS}	Gate-source voltage	$I_{Dq} = 10mA$	2.03	V
G_p	Power Gain	$P_{1dBcp}=38.9\ W$	29.4	dB
η_D	Drain Efficiency	$P_{1dBcp}=38.9\ W$	74.6	%

8. CW Performance Details

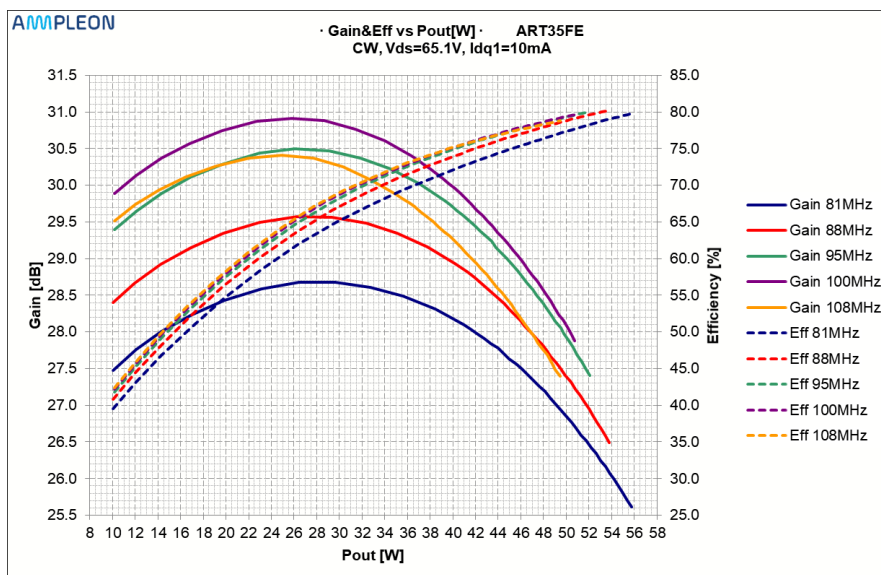


Figure 3 – Demo board CW performance

Table 4 – RF Performance overview

Freq [MHz]	Gmax [dB]	Pout@Gmax [W]	P1dB [W]	P2dB [W]	P3dB [W]	Effmax [%]	Pout@Effmax [W]	Eff P1dB [%]	Eff P2dB [%]	Eff P3dB [%]
81	28.67	26.38	44.68	50.93	55.54	79.82	55.78	74.70	77.74	79.71
88	29.57	26.26	43.22	49.18	53.53	80.24	53.80	75.66	78.47	80.15
95	30.50	26.08	41.60	47.44	51.73	80.05	52.07	75.71	78.35	79.94
100	30.92	25.83	40.48	46.34	50.66	79.60	50.77	75.40	78.01	79.57
108	30.41	24.89	38.92	44.94	49.40	78.84	49.47	74.62	77.26	78.81

9. User Guide

9.1 Biasing

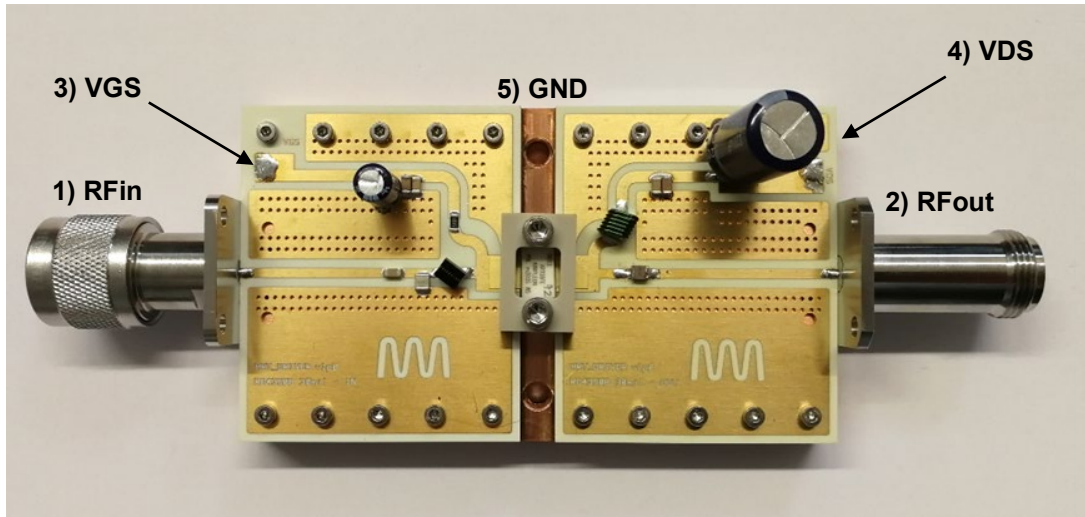


Figure 4 – Application board pin configuration

Table 5 – Pin description

Symbol	Pin	Description
RF _{IN}	1	RF input
RF _{OUT}	2	RF output
V _{GS}	3	Gate-source voltage
V _{DS}	4	Drain-source voltage
GND	5	Negative supply terminal for V _{DS} and V _{GS}

9.2 Bill of Materials

Table 6 – Bill of Materials

Part	Description	Value	Remark
C1, C5, C6	Multilayer ceramic chip capacitor	100 nF	100V
C2	Multilayer ceramic chip capacitor	56 pF	ATC800B
C3	Electrolytic capacitor	47uF	
C4, C7	Multilayer ceramic chip capacitor	4.7uF	100V
C8	Electrolytic capacitor	220 uF	100V
C10	Multilayer ceramic chip capacitor	1000 pF	ATC800B
R1	Chip Resistor	5.1 kOhm	1206
L1	Air core Inductor	100 nH	1812SMS
L2	Air core Inductor	90nH	2222SQ

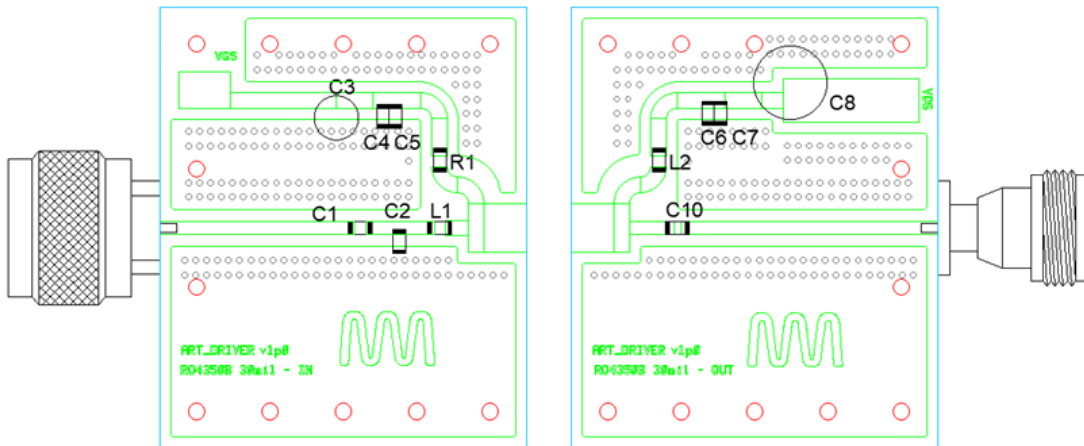


Figure 5 – Component mapping

9.3 Device markings

Table 7 – Module specifics

Parameter	Value
Manufacturer	Ampleon
Device	ART35FE
Comments	Engineering sample: PHL m2035 W5

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