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High Voltage RF LDMOS Technology for Broadcast Applications

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ABSTRACT

We present high voltage (40-50 V) RF LDMOS technologies to realize 300-500 W power levels for frequencies up to 1.0 GHz. This technology has an extremely good ruggedness, one octave wide band operation, and reliable circuit matching.

I. INTRODUCTION

RF power amplifiers are key components in base stations for personal communication systems (GSM, EDGE, W-CDMA, WiMAX). For these power amplifiers, RF Laterally Diffused MOS (LDMOS) transistors are the standard choice of technology because of their excellent power capabilities, gain, efficiency, linearity, reliability and low cost. LDMOS transistors are also the device choice in broadcast applications, where additional requirements like bandwidth, ruggedness, and thermal resistance are important.

In broadcast applications the bandwidth (BW) requirement is almost one octave for UHF: 470-860 MHz, more than a factor of 10 larger than for W-CDMA signals in base stations. Furthermore the LDMOS transistor should be designed to have, besides a VSWR of 10:1, the ability to withstand an abrupt mismatch in the transmitter at high power. The thermal resistance of the transistor and package is also very critical due to the high power levels requiring values below 0.4 K/W.

There is a continuous demand for higher power levels to reduce the transistor board space to a minimum. In order to develop a cost effective broadcast transmitter, twice the state of the art power (150 W) is required to make a direct 2 to 1 replacement of an analogue amplifier possible, while even higher power levels are desirable for digital broadcast signals. The maximum power is limited by the low impedance output-matching stage, giving problems with reproducibility and reliability. The way around is to develop a device, which can be operated at a higher supply voltage. This increases the load impedance making a more reliable circuit design possible, which ensures long lifetime of the matching components.

In this paper we present a 40 V LDMOS technology and the evolution to a 50 V technology. Both technologies have very wide band operation, extremely good ruggedness and very high output power for UHF broadcast applications. The power of these high voltage devices (300-500 W) has more than doubled compared to the state of the art 32 V LDMOS device.

II. DEVICE DESCRIPTION

The high voltage RF LDMOS technology is based on the base station RF LDMOS technology **[1]**. This technology, as shown in **Figure 1**, is processed in an 8-inch CMOS-fab capable of lithography down to 0.14 um, where the LDMOST process is derived from C075 CMOS (0.35 um gate) process with LOCOS isolation. Additions to this C075 process are the source sinker to the substrate, CoSi2 gate silicidation, tungsten shield, mushroom-type drain structure with thick 2.8 µm fourth AlCu metallization layer. The layout of the device is given in **Figure 2**. It consists of many (typically 50) parallel fingers connected by a drain and gate bond bar. Four of these dies are combined in a ceramic push-pull package to realize a power product.
A specially developed ESD device **[2]** protects the gate.

The breakdown voltage has further been increased to 90 and 110 V for the 40 V and 50 V, respectively, by engineering the drain extension, epitaxial layer thickness, and shield construction to open the way to high voltage operation.

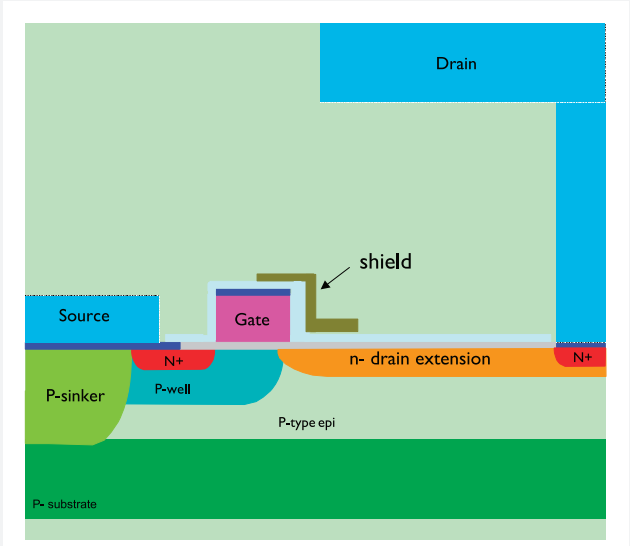

Figure 1: Schematic cross-section of state of art RF LDMOST fabricated in an 8 inch CMOS fab.

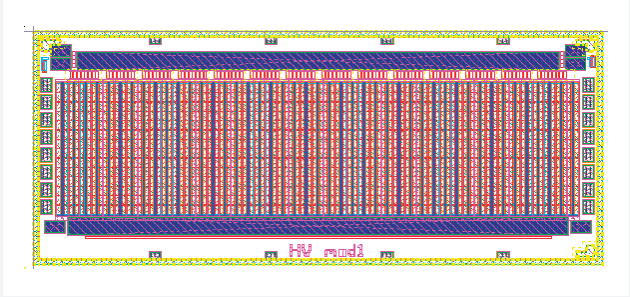

Figure 2: Top view of the layout of a single high voltage RF LDMOS device. Many finger are put in parallel to realize a 500 W power device.

The transistor has been designed to optimize the on-resistance and breakdown voltage. The success of this optimization can be recognized from the extremely flat electric field distribution across the drain extension region with only very weak peaks at the gate and drain edges. This distribution is shown in **Figure 3**. Also the ruggedness and reliability properties of the transistor radically improve due to this engineered field distribution.

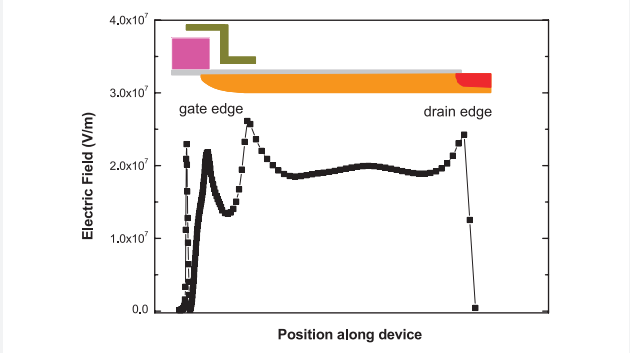

Figure 3: Simulated electric field distribution for the high voltage RF LDMOS technology at off-state breakdown.

III. RF PERFORMANCE

Figure 4 shows the narrow band CW class-AB RF performance of the high voltage LDMOS at 0.86 GHz for a supply voltage of 42 V. The gain of the device is typically 21 dB, being limited by a series gate resistor to achieve good stability for low frequencies and easy tuning. The peak-efficiency is 65 % at a power level of 400 W, while 500 W is achieved for the 50 V supply voltage technology (not shown).

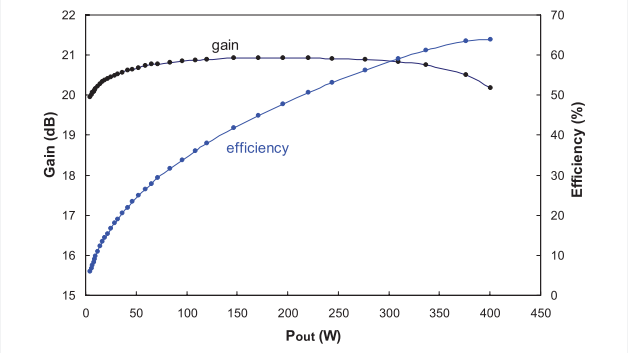

Figure 4: CW performance of the high voltage LDMOS transistor for a supply voltage of 42 V at a frequency of 0.86 GHz.

In **Figure 5** the 2-tone performance is plotted for a tone spacing of 100 kHz in a narrow band test fixture. The third order inter modulation product IMD3 crosses the -30 dBc close to 200 W average output power. The corresponding drain efficiency is 52 %.

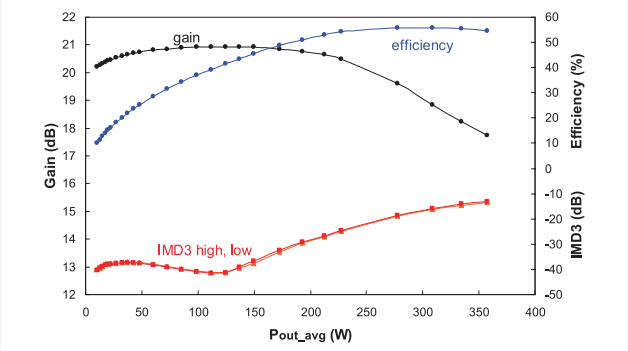

Figure 5: 2-tone performance at 0.86 GHz with a tone spacing of 100 kHz for a supply voltage of 42 V.

The broadcast industry is introducing digital broadcasting massively now, making broadcasters and service providers keen to push forward the move to digital transmission. This digital DVB-T signal is an OFDM modulated signal with a CCDF at 0.01 % probability of 9.6 dB (envelope approach). At the output of the transistor approximately 8 dB CCDF-0.01 % is required for linearization. The transistor should be able to handle both analog and digital signals. The device performance for DVB is shown in **Figure 6**. The shoulder distance for this signal (measured at 4.3 MHz from center frequency) stays below -32 dBc up to an average output power

of 85 W with a CCDF > 8 dB. The gain is about 20 dB and the efficiency is 32 %. For the 50 V technology 120 W output power is achieved and same efficiency.

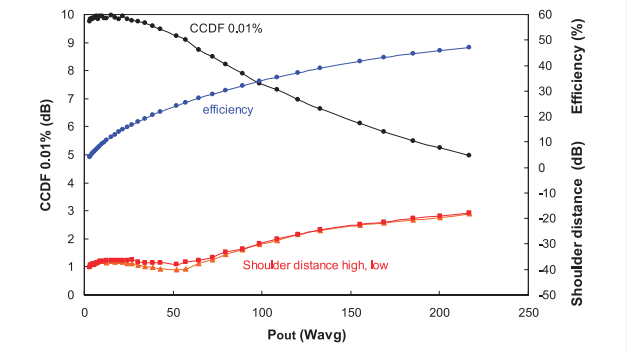

Figure 6: Performance at 42V for an 8k DVB-T signal.

IV. BROADBAND OPERATION

The broadband operation is measured for the push-pull transistor in a broadband water-cooled circuit. In order to achieve ultra wide broadband power, the device can internally be matched, as has been done for the 42 V technology. The broadband operation is shown in **Figures 7**, **8** and **9**. For CW operation the power levels for 1⁄2 dB compression are above 300 W. A broadband efficiency of 50-62 % is achieved.

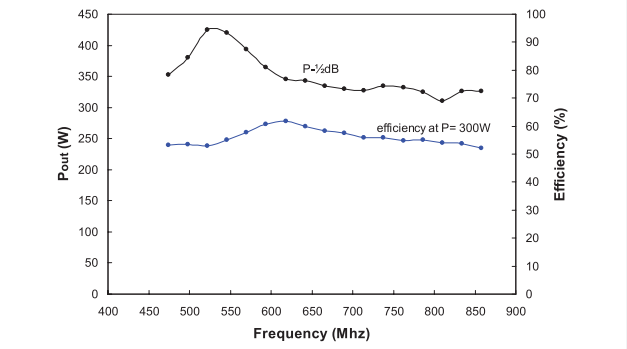

Figure 7: Broadband CW operation of the high voltage LDMOS showing the power at 0.5 dB gain compression and the efficiency at 300 W output power over the whole frequency band. Supply voltage is 42 V.

For 2-tone, the average power level at -30 dBc is far above 150 W in combination with an efficiency of 40-50 %. This results in a broadband linearity far below -30 dBc ensuring easy digital pre-correction.

The broadband device performance for DVB is shown in **Figure 9**. The DVB average power is more than doubled compared to the previous broadcast technology showing 75 W at 42 V and 110 W at 50 V with a CCDF of typically 8 dB. The efficiency is 30-32 % and the gain is 19 dB.

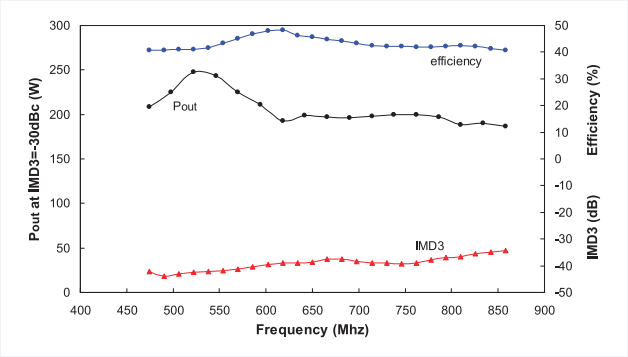

Figure 8: 2-tone power at an IMD3 of -30 dBc, gain, efficiency, and IMD3 versus frequency. Supply voltage is 42 V.

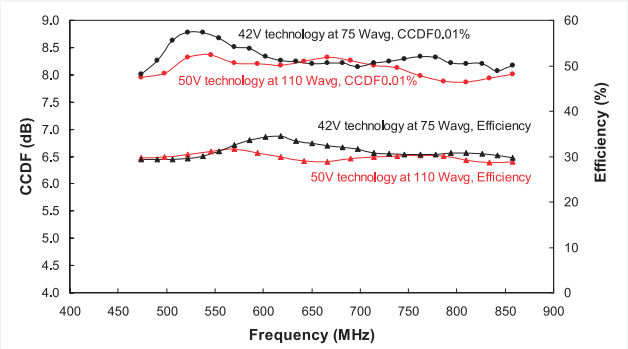

Figure 9: Performance of 42 V and 50 V technologies for an 8k DVB-T signal.

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V. RF PERFORMANCE ANALYSIS

From the series and parallel loss mechanisms **[1]** in the LDMOS we can analyze the realized measured DVB efficiency and compare this to the theoretical maximum efficiency in class-B. The maximum efficiency of the high voltage technologies is around 75 % at 0.86 GHz as deduced from measurement on small devices. The high voltage efficiency curve versus back-off power is plotted in **Figure 10** and we see that this curve is very close to the theoretical maximum class-B efficiency. The measured 30-32 % DVB efficiency is achieved at 8 dB back-off. At a frequency of 0.86 GHz and supply voltages of 40-50 V we have a combination of both parallel and series losses due to the on resistance and output capacitance. Based on their technology values we have estimated the losses in class-AB, which are indicated by the blue curve in **Figure 10**.

The realized efficiency is larger than is estimated from this loss mechanism theory. The difference can be attributed to higher harmonic contributions, which become important at low frequencies compared to the cut-off frequency.

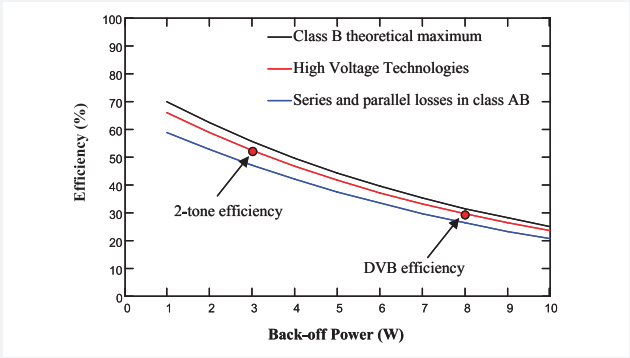

Figure 10: Efficiency versus power back-off for the high voltage LDMOS compared to the class-B theoretical maximum and a device modelled with series and parallel losses in class-AB.

VI. RUGGEDNESS

A crucial design requirement of the high voltage transistor for broadcast is the ability to withstand an abrupt mismatch at the output at full power. In this situation the transistor must be able to sink extremely large drain currents without fusing. In **Figure 11** a fast pulse I-V measurement for a small on-wafer test transistor (gate width Wg = 0.6 mm) is shown. It shows that the 42 V device can tolerate drain voltages up to 130 V, sinking a current of more than 0.4 A/mmWg before the parasitic bipolar transistor is triggered and the device breaks down. The 50 V device can withstand 150 V supply voltage peaks and sinks more than 0.8 A/mmWg. This extremely good ruggedness is confirmed by the ability to bias the transistor with supplies up to 60 V, far above the 40-50 V operation range. This superior ruggedness has been realized by tailoring the electric field of the high voltage technologies.

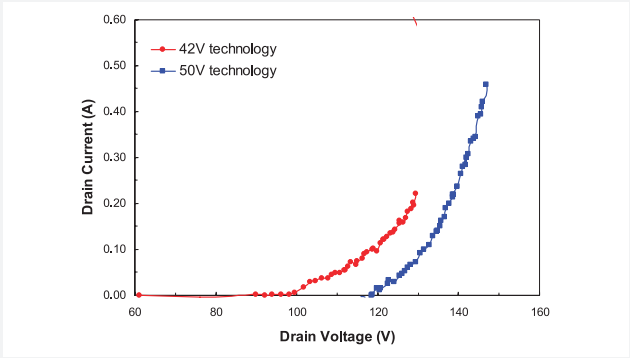

Figure 11: Pulsed drain current versus drain voltage measurements of 0.6 mm on-wafer 42 V and 50 V high voltage devices.

VII. RELIABILITY

The high voltage LDMOS process is qualified based on the standard procedures as used by Ampleon **[3]**, which comply with the standards of industry. Special attention is paid to the hot carrier degradation. Hot carrier degradation is caused by high electric fields in combination with high current densities. The degradation is measured while the transistor is biased to quiescent conditions, which is for the high voltage technology typically at a current of 5 mA per mm gate width and a drain-source voltage of 40-50 V. A degradation of this quiescent current could lead to a change in device performance. The high voltage device shows improved behaviour, which is shown in **Figure 12**. In the same plot there is degradation data of a broadcast transistor from a 32 V generation. Despite the higher bias conditions of the new voltage transistors, they show hardly any degradation. The degradation is only 2 % after an extrapolation to 20 years.

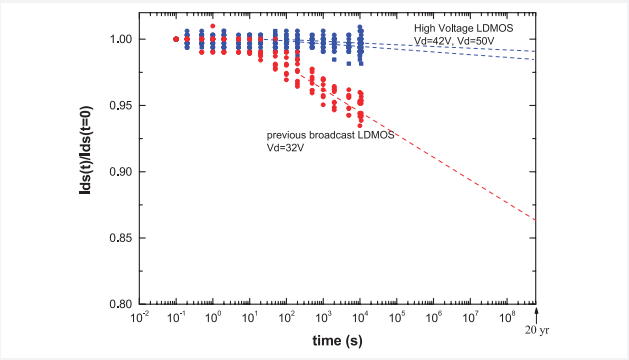

Figure 12: Degradation of the bias current as a function of time at room temperature. The high voltage LDMOS is biased at 42 V and 50 V, respectively. The previous broadcast LDMOS technology is biased at 32 V. The current in the bias points is 5 mA/mmWg.

The thermal resistance becomes very important for a 300-500 W device. So therefore the thermal resistance has been simulated using ANSYS **[4]**. An example of the simulation is shown in **Figure 13**. Using this ANSYS tool the thermal resistance of die and package was optimized. This has resulted in a typical measured value of 0.35 K/W, giving a junction temperature below 160°C allowing reliable operation.

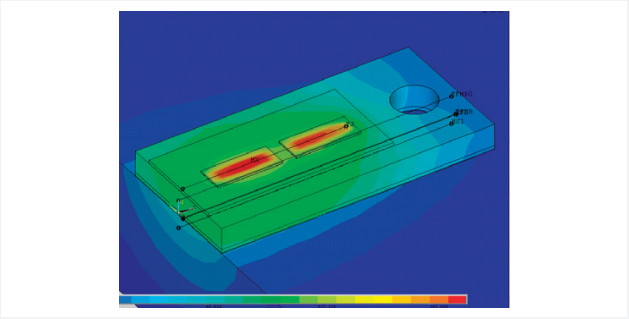

Figure 13: Thermal simulations with ANSYS have been done to optimise the thermal resistance of the high voltage LDMOS device. This figure shows one half of the power device.

VIII. CONCLUSIONS

To conclude, we have shown new high voltage (40-50 V) RF LDMOS technologies, which can deliver 300-500 W of CW power and 75-110 W of linear average DVB power for frequencies up to 1.0 GHz. These technologies have very good ruggedness, one octave wide band operation, and are extremely reliable.

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