AN11183

Mounting and soldering of RF transistors in overmolded plastic packages

Rev. 9 — 3 February 2025

Application note

Document information

Info	Content
Keywords	Overmolded Plastic (OMP) packages, heat sink, footprint, surface mount, reflow soldering, component handling, exposed heat spreader, SMDP, NSMDP
Abstract	This application note provides a general mounting recommendation/guideline suitable for plastic overmolded packages

Revision history

Rev	Date	Description
AN11183#9	20250203	Overall revision
AN11183#8	20242406	Overall revision
AN11183#7	20231408	Added LGA12x8 in Table 5.
AN11183#6	20230127	Modifications: • Chapter 4.1.1 added info for PQFN, increase solder volume in some cases.
AN11183#5	20220915	Modifications: • Table 1 range 150 µm to 200 µm (was 150µm). • Table 5 added packages DFN 7x6.5, DFN 4.5x4 and OMP1.
AN11183#4	20220202	Modifications: • Chapter 3.1.1.1, Heatsink cavity; added Fig.14 • Chapter 6, Reflow solder process; added three phase explanation. • Chapter 6.2, updated table 5
AN11183#3	20190627	Overall revision, include new package platforms: PQFN/LGA.
AN11183#2	20160302	Modifications: • The format of this document has been redesigned to comply with the new identity guidelines of Ampleon. • Legal texts have been adapted to the new company name where appropriate.
AN11183#1	20121106	Initial version.

Contact information

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1. Introduction

1.1 General (mounting recommendations RF power)

This document is intended to guide and advice customers in ways how to solder overmolded packages RF Power transistors. Each customer has its own way of designing application boards and assembly of the devices, so therefore not possible to cover all specific requirements.

1.2 Definition

The following words in this document:

- “Heat sink” refers to the heat sink located under the PCB, the application heat sink forms the part of the thermal path that carries heat away from the device to the cooling air.
- “Exposed heat spreader” or flange refers to the exposed metal underneath the plastic over molded devices (or Cu base), is designed for attachment to the customer board.
- “Printed Circuit Board (PCB)” refers to the electrical interconnection between the RF power devices and other electrical components that are part of a PA.
- "Foot Print or Solder land" refers to the area on which to solder the device.

1.3 Main product groups

The IC package provides a means for connecting the package to the external environment, such as printed circuit board, via leads, lands, balls or pins; and protection against threats such as mechanical impact, chemical contamination and light exposure. Additionally, it has a key role to dissipate heat produced by the device.

This document covers the different overmolded packages families offered by Ampleon, grouped by lead and leadless packages.

1.3.1 Lead packages

1.3.1.1 OMP

Overmolded Package (OMP) is a lead frame based plastic package having leads protruding from the side portion of the package and a bottom metal flange for high-power thermal dissipation.

Straight leads devices are designed to be reflowed into a cavity with the source contact soldered to a pallet or coin and the leads soldered to the PCB, gull wing versions are designed for customers using surface mount assembly.

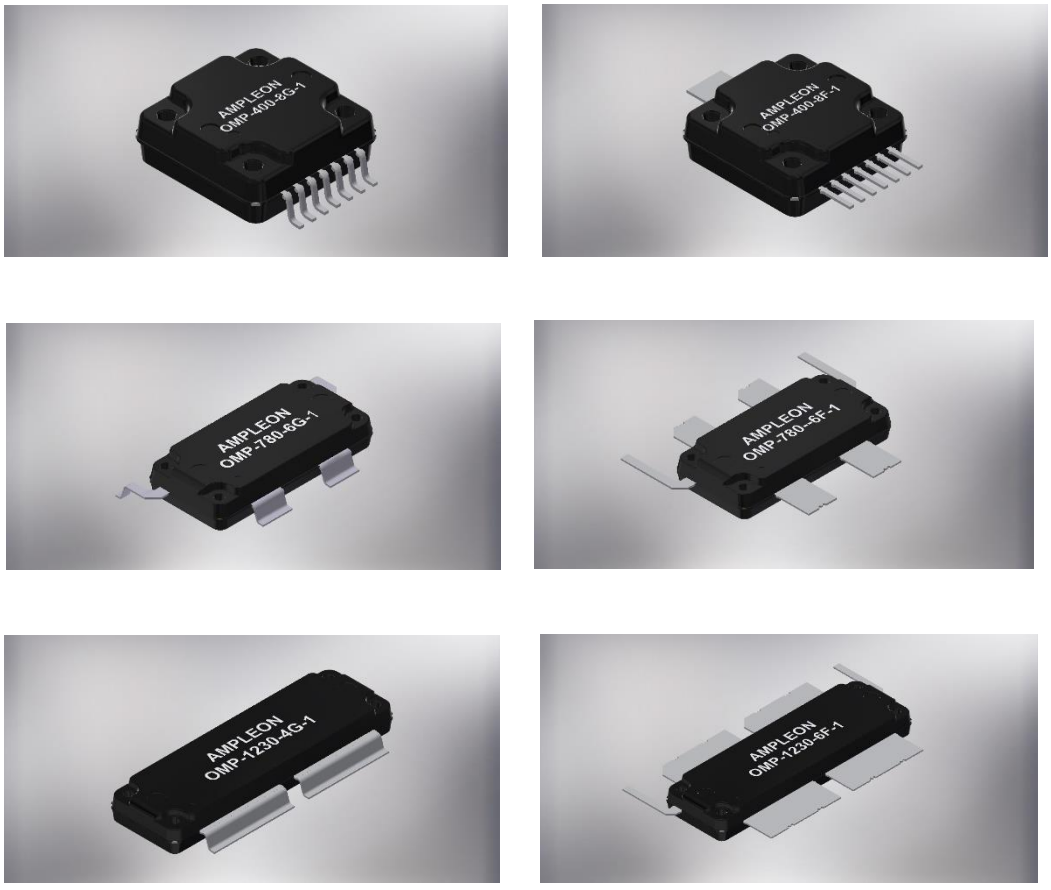

Figure 1. Typical OMP packages gull wing and straight leads versions

1.3.1.2 TO

Smaller version of OMP package

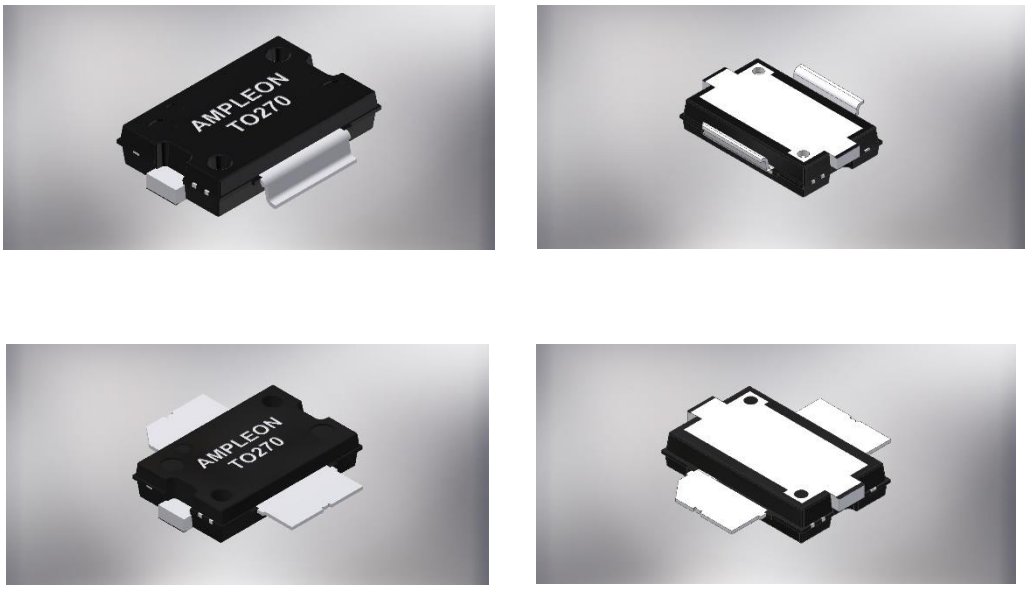

Figure 2. Typical TO package; gullwing and straight leads versions; top and bottom view

1.3.2 Leadless packages

1.3.2.1 PQFN

Power Quad Flat No-Lead (PQFN) is designed primarily for board-mounted power applications. Instead of leads, it uses metal lands around the periphery of the bottom of the package body for electrical connection to the outside world, includes large planes for grounding and high-power thermal dissipation.

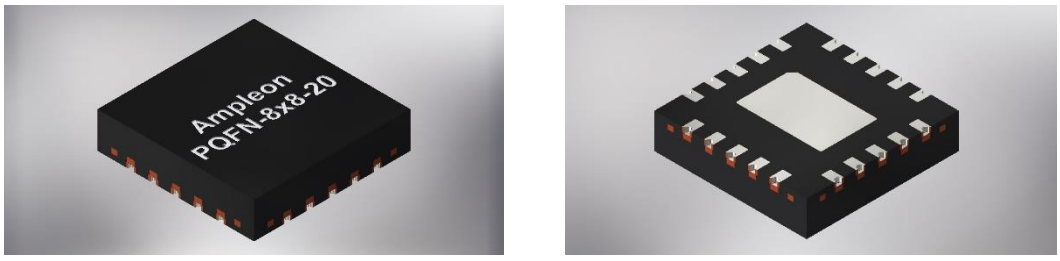

Figure 3. Typical PQFN package top and bottom view

1.3.2.2 HVSON (DFN)

Dual flat no leads, similar to Quad Flat No-Lead (QFN), except that the latter has lands all around the periphery of the package instead of just two sides like the DFN.

Due to its lower package thickness it’s intended for lower power applications.

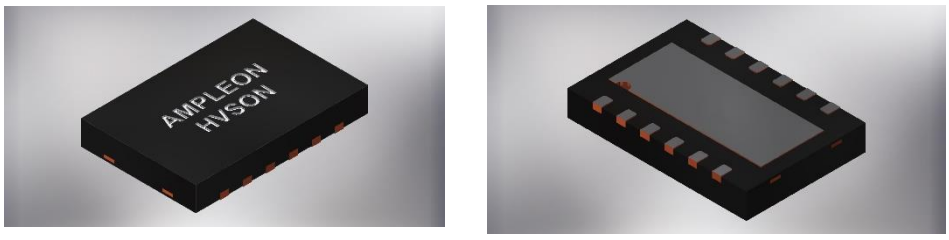

Figure 4. Typical HVSON package top and bottom view

1.3.2.3 LGA

Land grid array (LGA) packages is a surface mount device. These are leadless packages with electrical connections made via lands on the bottom side of the component to the surface of the connecting substrate (PCB). The LGA is typically made with overmolded organic laminate as substrate with ENEPIG (Nickel-Palladium-Gold)-plated terminals.

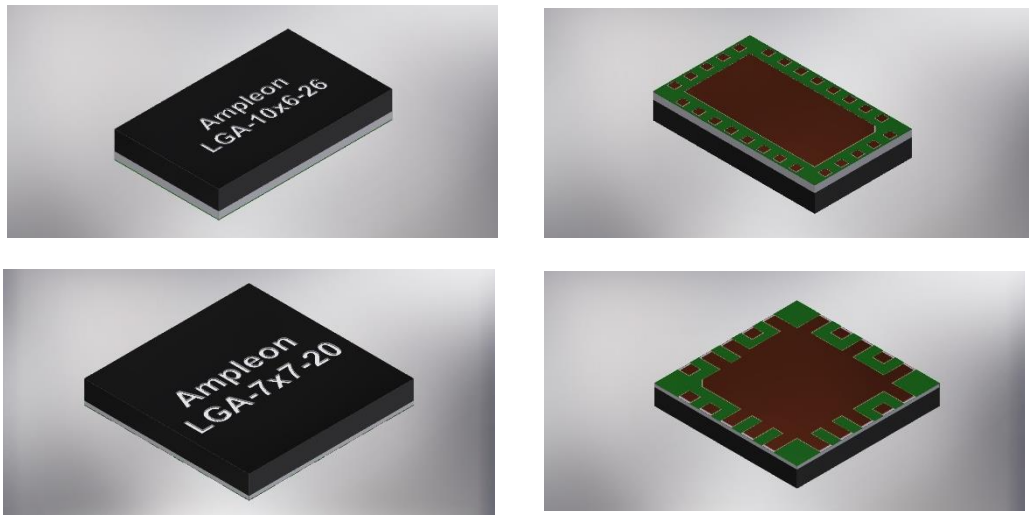

Figure 5. Typical LGA packages, top and bottom view

2. Application board

Types of boards

Depending on the power management, and device type there are number of different configurations, below some of the most common ones.

2.1 Lead packages

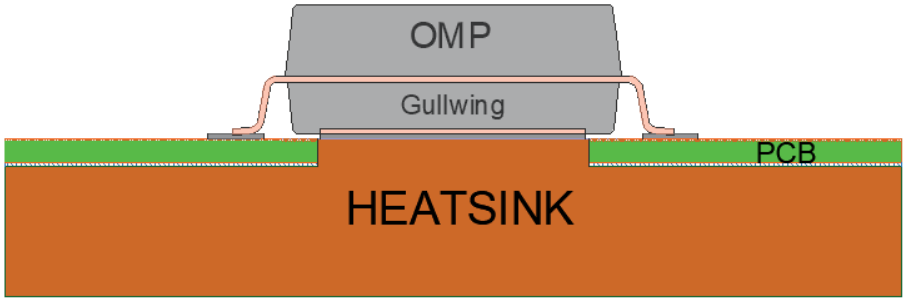

Figure 6. PCB bonded to a heat sink with a pedestal, intended for gullwing high-power packages

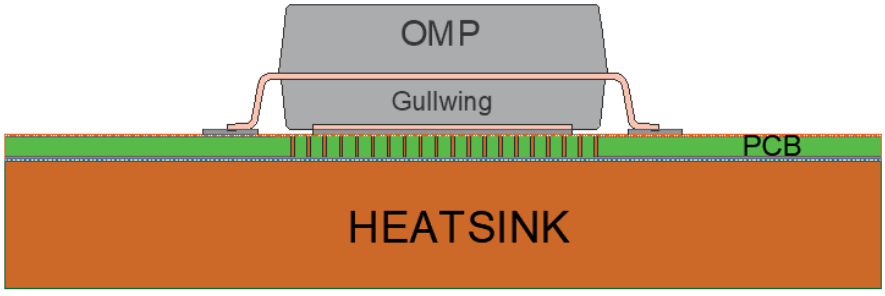

Figure 7. PCB with vias bonded to a heat sink, intended for gullwing low power packages

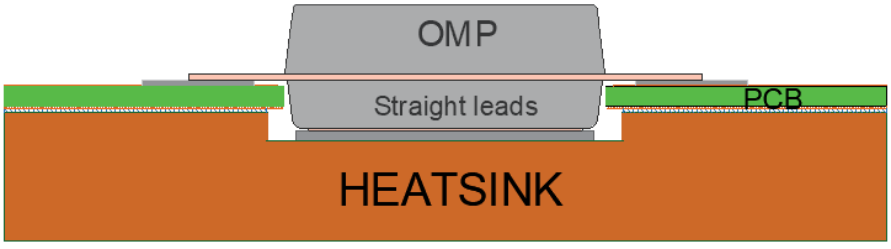

Figure 8. PCB bonded to a heat sink with a cavity, intended for straight leads package

2.2 Leadless packages

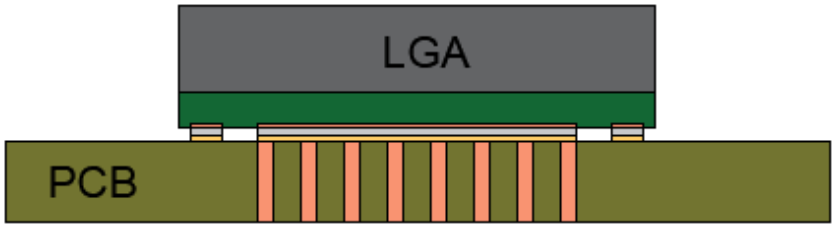

Figure 9. PCB with vias

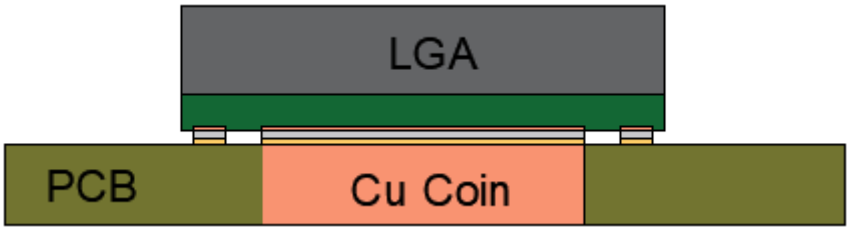

Figure 10. PCB with embedded Copper coin

3. Board Design

3.1 PCB land pad design

Design should satisfy requirements for electrical, thermal and reliability performance, board level assembly and board level testing.

The dimensions given in this section are for the solderable portion of the PCB /package.

3.1.1 Straight leads packages

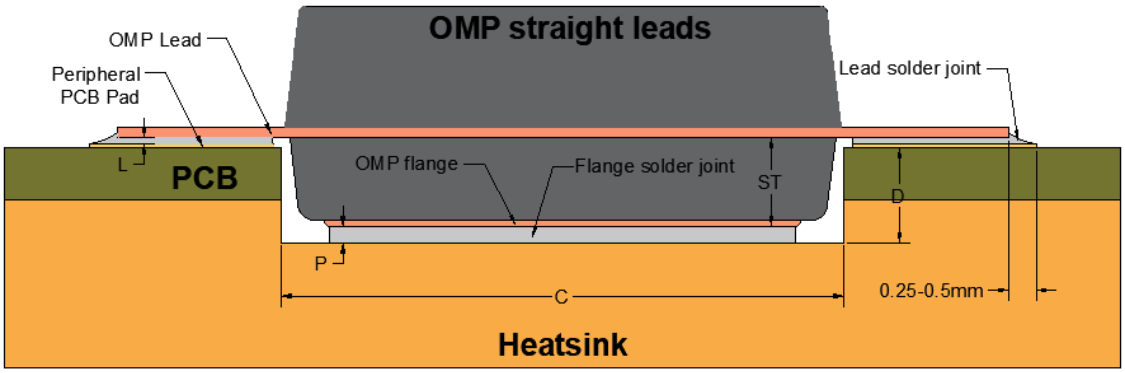

Figure 11. OMP straight leads package cross section view

Looking to the cross section view of an OMP package (Figure 12) we recommend the outside edge of the solder pad should be longer than the outside tip of the leads by a minimum of 0.25 mm.

The pad area should be at least 0.15 mm from the edge of the cavity (pull back), PCB manufacturer should provide a design rule on this dimension.

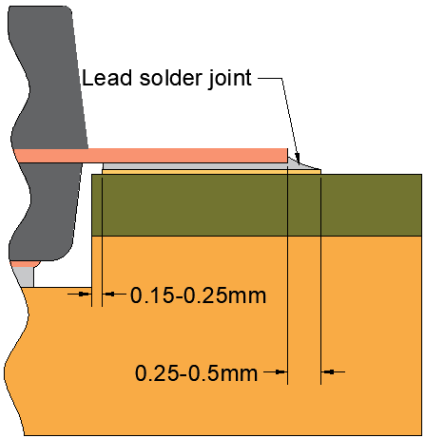

Figure 12. OMP straight leads package cross section view detail

3.1.1.1 Heatsink cavity

The heat sink design depends primarily on dissipated heat and on the other components located on the PCB. These vary from one application to another, therefore no general recommendations on the size and thickness of the heat sink.

The package body is placed through an aperture in the PCB onto the heat sink.

The dimensions of the aperture in the PCB should be such that the package can be easily inserted through it by manual or automatic processes.

Cavity width/length opening (C, Figure 13).

C= Nominal cavity aperture dimension (X&Y directions) = Maximum molded body size + Pick & Place placement capability + cavity tolerance/2.

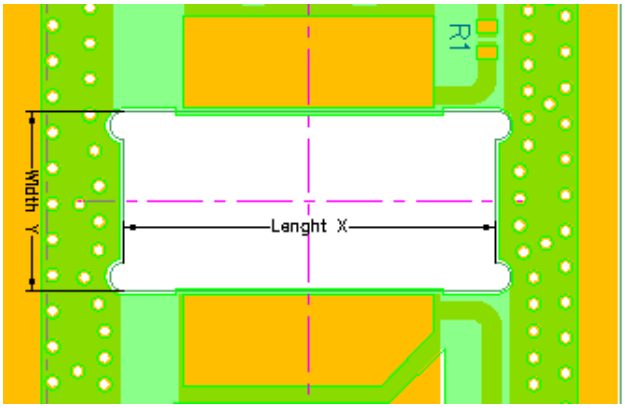

Figure 13. PCB Cavity aperture X & Y directions

Heatsink cavity depth Figure 14.

Heatsink cavity depth (D) = Package Stand off (ST) + Preform thickness (P) – solder thickness under lead (L) - Gap lead to solder before reflow (G).

Typical recommended values:

- Preform thickness (P) = 200 - 400 microns.
- Solder thickness under lead (L) = 150 microns.
- Gap lead to solder before reflow = 0 to 100 microns.

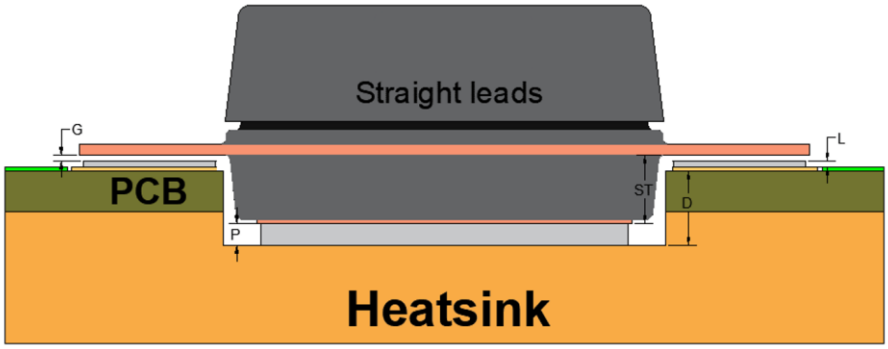

Figure 14. Heatsink cavity depth

Due to its importance factor on product performance and product reliability this dimension tolerance should be minimized as much as possible, Ampleon recommends a maximum cavity depth tolerance of +/- 0.08 mm.

We also advice to limit bottom surface roughness (Ra < 6 microns).

All of these parameters will vary due to their tolerances. Determining the cavity depth is a simple calculation of a worst-case tolerance stack up; however it might end up in a value simply too large for normal production (the leads will likely lay too high above the PCB).

A more common approach is to make use of the Square Root of Sum of the Square method. Use the actual distribution of all valid parts, in case these are not available take the actual specification.

3.1.2 Gull wing leads packages

Looking to the cross-section view of an OMP gullwing package (Figure 15) we recommend to extend PCB heel and toe extensions pads 0.25 to 0.50mm, this will allow a good filet at both sides of the lead.

A larger heel pad may cause an excess solder condition on the inside of the lead reducing flexibility and increasing stresses on the solder joint.

Pad width should be approximately 60 % of the lead pitch, in case of single lead, PCB pad should be extended 0.125mm to both sides.

Soldering of Gullwing package should ensure proper contact on the governing interfaces. Solder thickness on pad and leads should consider the package's outline drawing tolerances such as Seating plane, Lead angle and Gauge plane as presented in Figure 16. Force application during attachment and/or soldering jig may also help to ensure

proper contact on the governing interfaces.

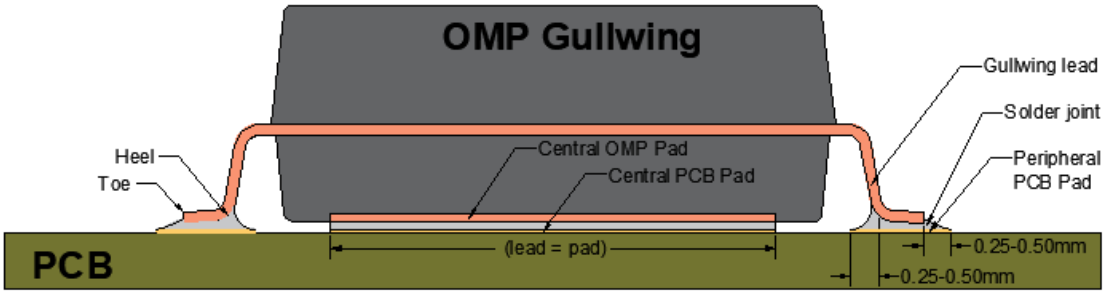

Figure 15. Cross section view of an OMP GW package

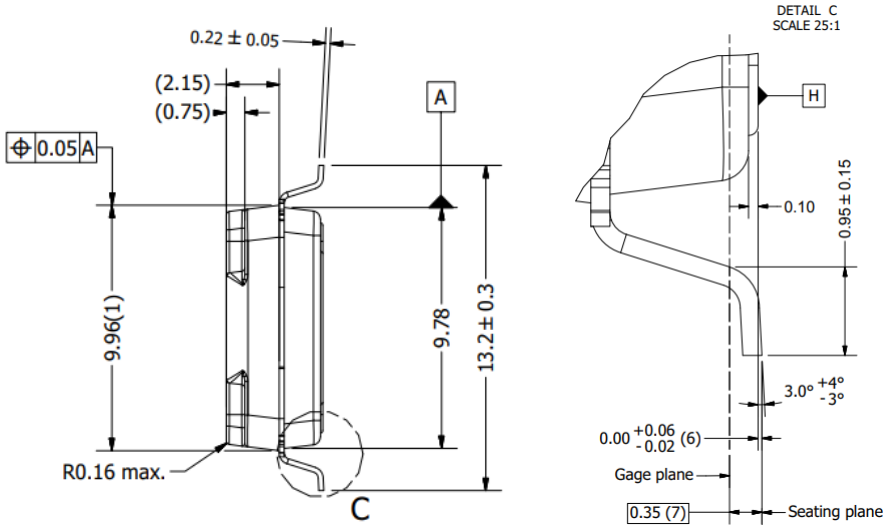

Figure 16. Package outline drawing of OMP GW package.

3.1.3 Leadless package

Design considerations:

- Good symmetry of the leads and pads so that the device can self-center on the pad layout.
- Maximize center pad size, close as possible to maximum value of the exposed pad on the package.
- Allow enough distance between the peripheral pads (0.15 mm minimum recommended) to accommodate the solder mask. This will prevent shorting between two pads or between two leads.
- Electroless Nickel, Palladium immersion Gold (ENEPIG) is the preferred surface finish for the PCB land pads.
- Place as many as possible thermal vias to connect the top and bottom ground copper planes in the PCB under the RF ground pad. Effectiveness of thermal vias diminishes when they are placed farther from the package ground pad.

3.1.3.1 PQFN/HVSON/DFN

The pad layout includes the design of both the center pad and peripheral pads.

Looking to the cross section view of a PQFN package (Figure 17), we recommend extending PCB peripheral pads 0.1 to 0.25mm. This may form a solder fillet below 30% of the sidewall and may also help in minimizing the solder voids. Looking to the front view (Figure 18), we recommend extending the peripheral pad width by 0.025mm to both sides.

Solder mask opening length (when applicable) = PCB land length + 0.1 mm (depending on PCB supplier design rules).

These recommendations are provided as a guideline and may require some fine-tuning for a specific application or process.

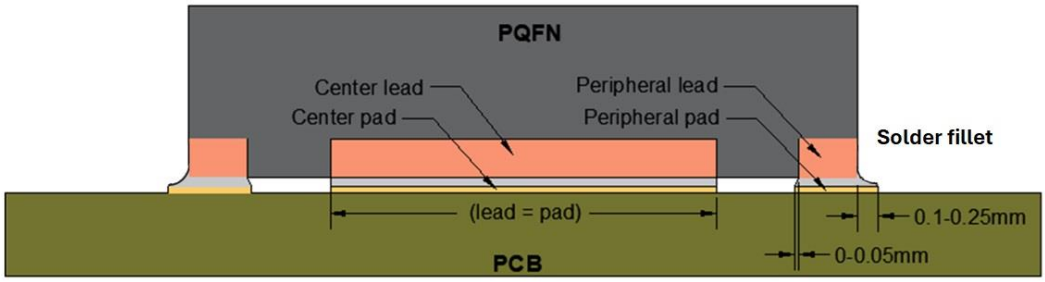

Figure 17. Cross section view

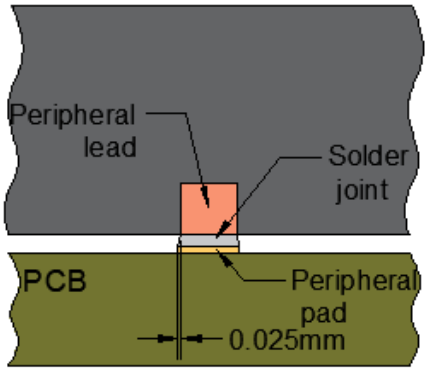

Figure 18. Front view of solder joint

3.1.3.2 LGA

LGA footprints may be similar to ones used on a Power Quad Flat Pack No-Lead (PQFN) package.

The solderable area on the mother board should match the nominal solderable area on the LGA package (1:1 ratio) (Figure 19).

NSMD land is recommended to maximize solder joint life.

Solder mask opening length (when applicable) = PCB land length/width + 0.1 mm (depending on PCB supplier design rules).

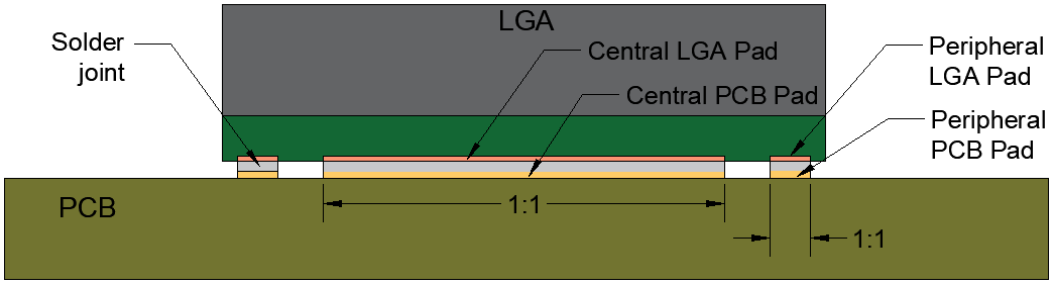

Figure 19. Cross section view

3.2 PCB land pattern solder mask

The industry has two common concepts on the opening of solder resist:

- Non solder mask defined (NSMD) the solder mask openings are larger than the exposed metal pad (Figure 20).
- Solder mask defined (SMD) the solder mask overlaps the underlying metal pad, which is slightly larger than the solder mask opening (Figure 21).

Selection of NSMD versus SMD should be based on complexity of the board design and board supplier capability for solder mask registration and tolerance.

Solder mask design should follow PCB manufacturer design rules, typically the copper to solder mask and solder mask overlap is 0.075 mm.

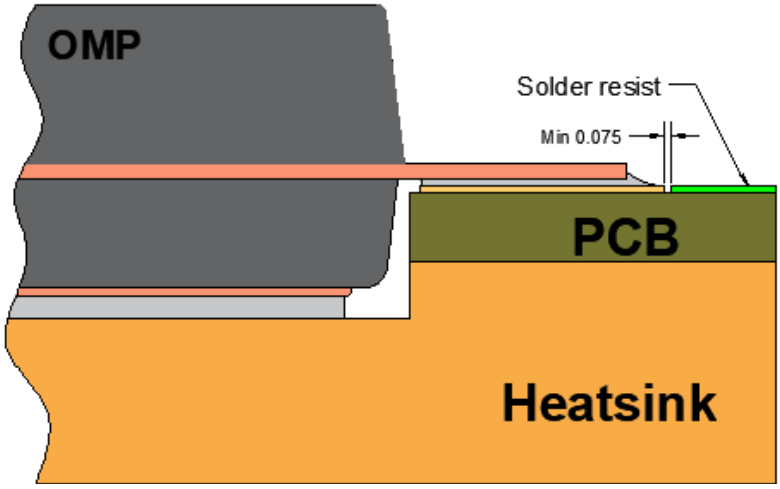

Figure 20. NSMD cross section view OMP straight leads package

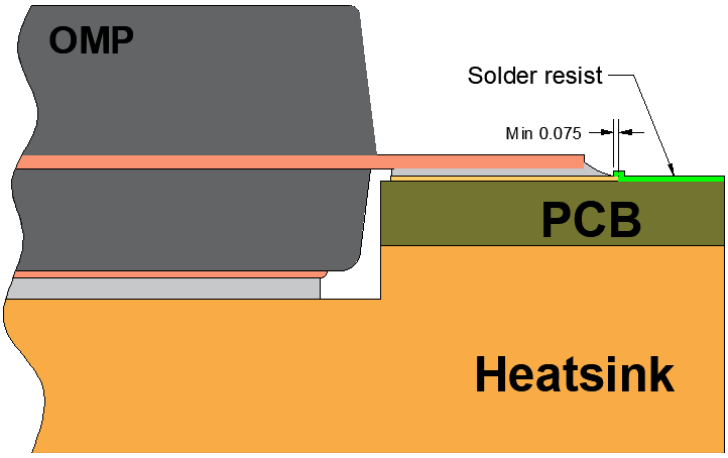

Figure 21. SMD cross section view OMP straight leads package

Even if the metal pad on the PCB extends beyond the dimensions, it is recommended that a solder mask dam is used to define the solderable area for the lead (Figure 22). This prevents the solder overflow from the lead and wetting the remaining trace

Minimum recommended dam width is 0.2mm.

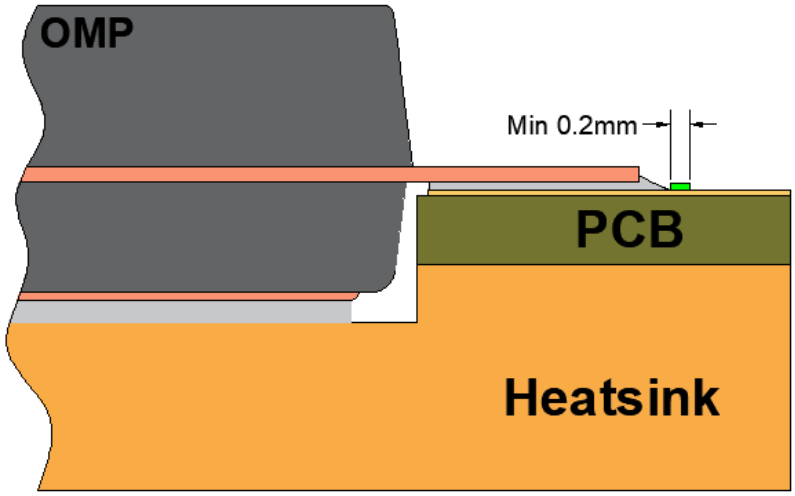

Figure 22. Solder mask dam cross section view OMP straight leads package

4. Solder paste printing

For applying solder paste you can use either stencil or silk screen printing techniques taking care of standard process control. The aperture dimensions, that is, the length and width and the depth (the stencil thickness) should be made fit for each package type and balanced according the used stencil thickness. Stencil thickness is dictated by all components on the board. The aperture length and width should be selected such that it fits the stencil process.

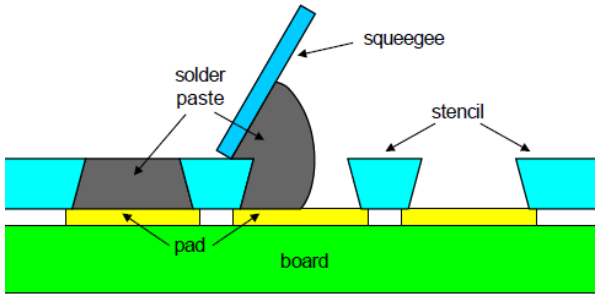

Figure 23. Stencil printing

4.1 Stencil thickness

It is possible to use a stencil that has a different thickness at different locations, an example of this is the step-stencil. This, however, is only recommended if there is no other solution.

Stencils (Figure 24 Stencil example) are commonly made from metal Nickel alloy; they may be either electro-formed or laser-cut (preferred). Typical stencil thickness is given in Table 1.

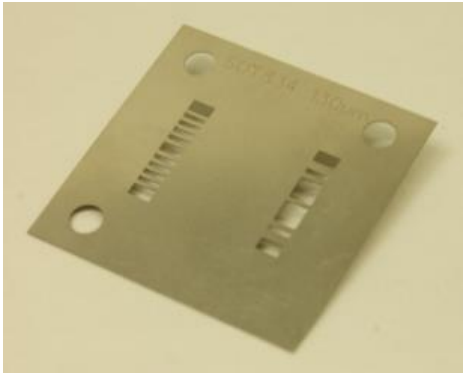

Figure 24. Stencil example

Table 1. Typical stencil thickness

Semiconductor package pitch	Stencil thickness
≥ 0.5 mm	120 μm to 200 μm
0.4 mm to 0.5 mm	100 μm to 125 μm

In most cases, the package will be mounted on a PCB after the rest of the substrate has been populated. A typical process flow includes:

- Solder paste printing.
- Solder preform placement (where required).
- Component placement (including the OMP package).
- Reflow.
- Inspection.

The height of the solder on the PCB pads will depend on the stencil that was used for printing. Low stencil thickness may also help in minimizing the solder voids.

4.1.1 Aperture size

Another parameter in the stencil design is the aperture size.

Typically, the stencil apertures are 25µm smaller than the solder lands on all sides. In other words, the solder paste lays 25µm inward from the solder land edge. This usually results in stencil aperture dimensions that are 50µm smaller than the corresponding solder land dimensions.

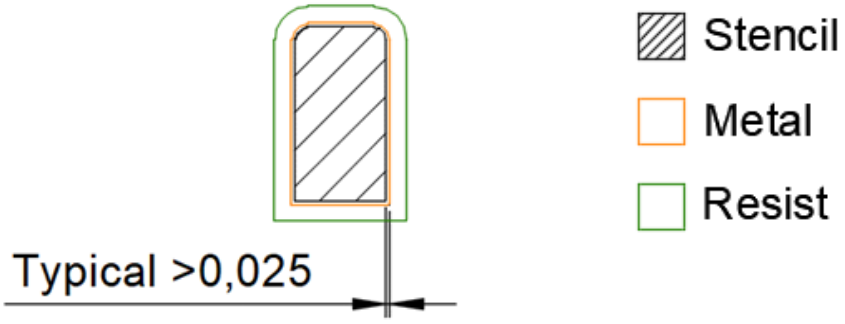

Figure 25. Solder print to land dimension for NSMDP

One can deviate from above recommendation, for PQFN in some cases stencil apertures size can be designed to a similar dimension or slightly larger as the solder lands size in order to increase the solder volume. Also increasing the stencil thickness can be considered.

With very large solder lands, such as printing solder paste on a heat sink land as used for PQFN and LGA, it is advised to print an array of smaller solder paste deposits, these deposits cover approximately 50-80% of the total heat sink land area. It is also advised to keep the solder paste away from the edges of this land. This concept combined with other important factors (solder paste, reflow profile setting and stencil thickness) will allow flux to outgas properly and may help minimize the solder voids.

The solder paste pattern for the leads (IO's), should have same coverage ratio as the large solder land. A paste-printing pattern for exposed die pads is illustrated by the example shown in Figure 26.

A PQFN 7x7 with an exposed pad of 4.8 mm x 4.8 mm, for example, can have sixteen solder paste deposits that are arranged in a four-by-four array. The solder paste deposits are 0.85 mm x 0.85 mm, at 1.25 mm pitch.
This way, the solder paste area is 16 x (0.85 mm x 0.85 mm) and dividing this by the exposed pad area 4.8 mm x 4.8 mm yields a solder paste coverage of approximately 50 % of the total pad area.

The land area in this example is 0.05mm larger on all 4 sides.

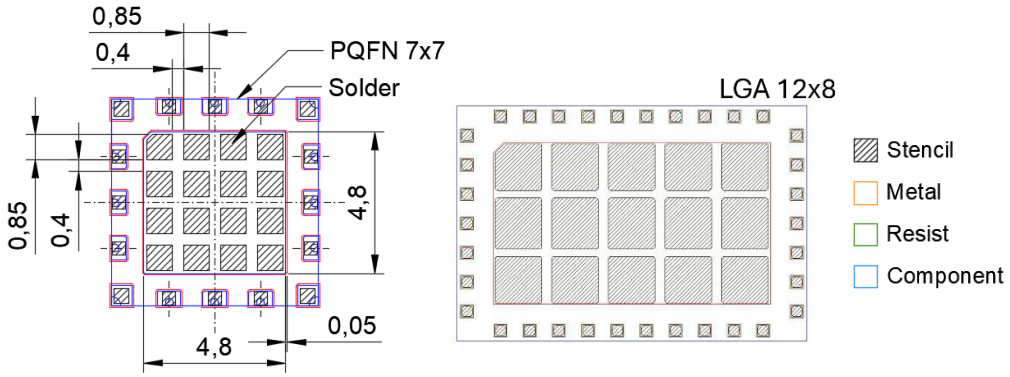

Figure 26. Example of Solder paste dimensions on the land area for a large die pad

When designing a footprint in NSMDP or SMDP, there is no difference in stencil lay-out.

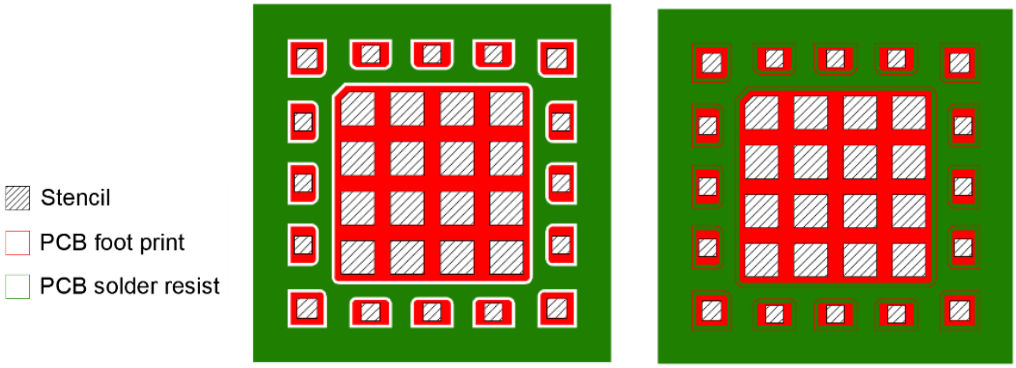

Figure 27. Solder paste printing on NSMDP (left) and SMDP (right)

No-clean flux solder paste and no-clean flux solder wire should be used, so the PCB and the package do not have to be cleaned after reflowing or manual soldering.

The footprint design describes the recommended solder land on the PCB to make a reliable solder joint between the semiconductor package and the PCB.

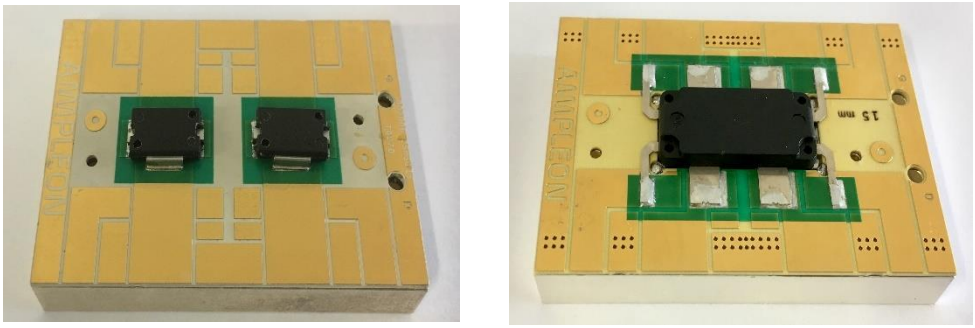

Figure 28. Examples of soldered gull wing and straight leads devices

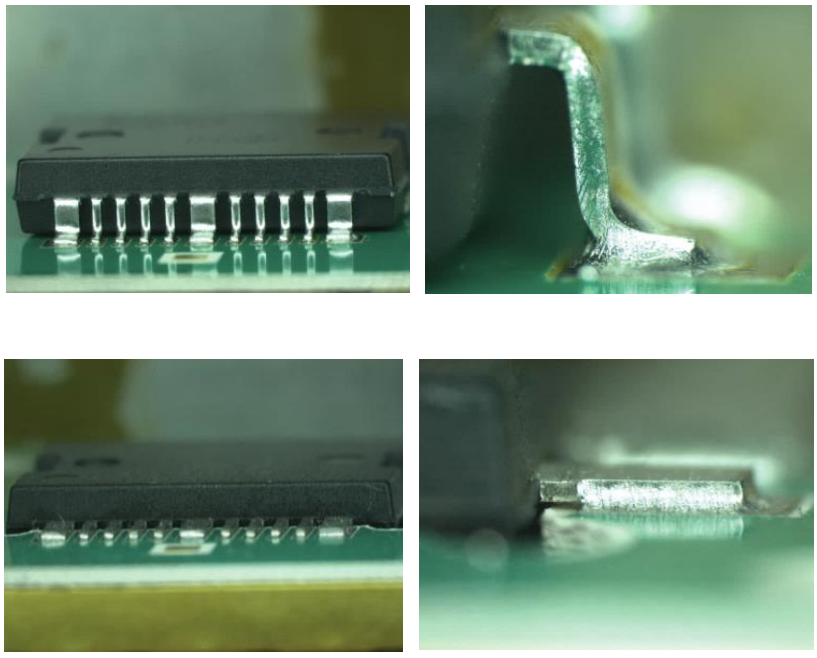

Figure 29. Close up of soldered gull wing and straight leads devices

Common board finishes include NiAu, Organic Solderability Preservative (OSP), and immersion Sn. Although finishes may look different after solder reflow process, and some appear to have better wetting characteristics than others, all common finishes can be used, provided that they are in accordance with the specifications. Examples of other issues in board quality are (i) tolerances on the pad and solder resist dimensions and component placement, (ii) maximum board dimensions, and (iii) flatness. The application board is usually a mix of large and small components together with thermal design features. In board designs where large components or thermal design features are in close proximity to small components, solderability issues may arise (i.e. hotspots).

5. Solder materials

Solder paste and performs are the most common materials used for soldering of lead packages, Table 2 gives recommendations of the possible combinations.
Leadless packages use only solder paste.

Table 2. Overview of solder pastes and preforms used

Solder type	Gull Wing		Straight Leads	
	Leads	Heat spreader	Leads	Heat spreader
Solder paste	X	X	X	-
Solder preform	-	X	-	X

5.1 Solders

In line with European legislation, it is recommended to use a Pb-free solder paste or preform, although exemptions are granted for selected applications.

A wide variety of Pb-free solder pastes are available, containing combinations of tin, copper, antimony, silver, bismuth, indium, and other elements. The different types of Pb-free solder pastes/preforms have a wide range of melting temperatures.

As a substitute for SnPb solder, the most common Pb-free paste/preforms used is SAC, which is a combination of tin (Sn), silver (Ag), and copper (Cu). These three elements are usually in the range of 3 to 4 % of Ag and 0 to 1 % of Cu, which is near eutectic. SAC typically has a melting temperature of around 217 °C, and it requires a reflow temperature of more than 235 °C (Table 3).

Table 3. Minimum peak temperature for soldering per alloy (JEDEC J-STD-020)

Solder	Melting temperature	Minimum peak reflow temperature (measured at the solder joint)
SAC	217 °C	235 °C
PbSn	183 °C	215 °C

Care should be taken when selecting a solder and note that solder types are categorized by solder sphere size. For small packages or fine pitch applications solder paste type 3 or better are recommended.

A no-clean solder paste or preform does not require cleaning after reflow soldering and is therefore preferred, provided that this is possible within the process window. If a no-clean paste is used, flux residues may be visible on the board after reflow.

Ampleon advises using a preform with pre-applied flux for flange to heat sink attachment. It reduces voids and ensures the required amount of solder. Preforms with pre-applied flux are available in the market.

In case separate flux (manually, like with a brush, pen or dipping) is applied in combination with a preform, extra care needs to be taken not to use excessive amounts of flux. These might increase the chance of voids in the solder joint.

For more information on the solder paste and solder preforms, please contact your solder supplier.

6. Reflow soldering Process

Ampleon advises to use a convection oven rather than a conduction or radiation oven. A convection oven provides a uniform heat and a very controlled temperature (± 2°C). Moreover, it allows soldering a wide range of products due to the temperature uniformity. During the reflow soldering process, all parts of the board are subjected to an accurate temperature/time profile.

A temperature profile essentially consists of three phases:

- **Pre-heat:** the board is warmed up to a temperature that lies lower than the melting point of the solder alloy.
- **Reflow**: the board is heated to a peak temperature well above the melting point of the solder, but below the temperature at which the components and boards are damaged.
- **Cooling down:** the board is cooled down, so that soldered joints freeze before the board exits the oven.

The peak temperature during reflow has an upper and a lower limit.

6.1 Lower limit of peak temperature

The minimum peak temperature must be high enough for the solder to make reliable solder joints. This is determined by solder paste characteristics; please contact your solder paste supplier for details.

6.2 Upper limit of peak temperature (Body related)

The maximum peak temperature must be lower than the temperature at which the components are damaged. This is defined by MSL testing of the package. The maximum body temperature during reflow soldering depends on the body size and on the demand to respect the package MSL.

The maximum allowed body temperature depends on the package dimension and should be in accordance with the JEDEC recommendations.

Table shows the classification temperature (Tc) for a Pb-free process according to JEDEC J-STD-020 (Moisture/Reflow Sensitivity Classification for Non-hermetic Solid-State Surface Mount Devices).

Table 4. JEDEC J-STD-020 – Classification temperature (Tc) for a Pb-free process

Pb-Free Process - Classification Temperatures (T_c)

Package Thickness	Volume mm^3 <350	Volume mm^3 350 - 2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm - 2.5 mm	260 °C	250 °C	245 °C
>2.5 mm	250 °C	245 °C	245 °C

classification temperature (T_c) – The maximum body temperature at which the component manufacturer guarantees the component MSL as noted on the caution and/or bar code label per J-STD-033.

The package thickness and dimension can be obtained in the package's outline drawing. The recommended maximum body temperature is published in Ampleon's website documentation.

6.3 Upper limit of peak temperature (Board related)

The maximum peak temperature must be lower at which the boards are damaged.

This is a board characteristic; please contact your board supplier for details.

6.4 Reflow Profile

The second phase in the reflow profile is the reflow zone, in which the solder melts and forms soldered joints. The minimum peak temperature, in which all solder joints in the cold as well as the hot spots must reach, depends on the solder alloy. However, no region on the board may surpass a maximum peak temperature, as this would result in component and/or board damage. Even if the cold and hot spots start the reflow phase with roughly the same temperature, the hot spots will reach a higher peak temperature than the cold spots. Yet, both the hot spots and the cold spots must lie within the allowed peak temperature range. This may require some tweaking of the oven temperature settings and conveyor belt speeds. In extreme cases, even the board layout may have to be optimized to limit the temperature difference between the cold and the hot spots.

When reflow soldering, the peak temperature should never exceed the temperature at which either the components or the board are damaged. For reflow soldering with SAC, the peak temperature should be larger than 235 ºC.

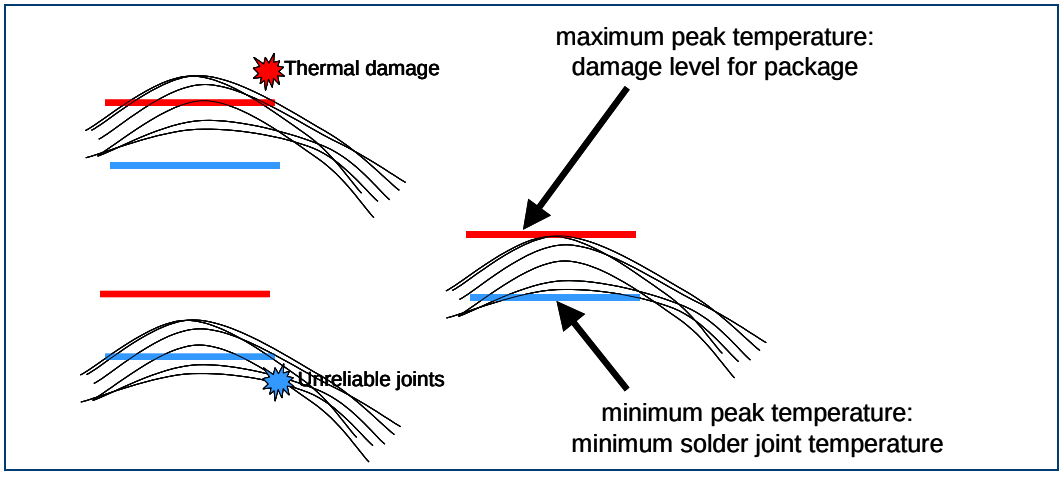

Figure 30. Fitting both the hot and cold spots into the required peak temperature range

The black lines in Figure 30 represent the actual temperature profiles for a number of different spots on a board. The bottom line represents the cold spot, and the top line corresponds to the hot spot. The blue line represents the minimum allowed peak temperature and the red line is the maximum allowed peak temperature. At the top left, some regions on the board are exposed to temperatures that are too high, resulting in damage. At the bottom left, some regions on the board are exposed to temperatures that are too low, resulting in unreliable joints. At the right, all of the regions on the board have peak temperatures that fall within the upper and lower limits.

6.5 An example of a reflow profile using SAC solder:

The reflow soldering profile should be calibrated with a thermocouple glued under the device to prevent a temperature offset.

Peak temperature in any of package main parts (leads, flange, and cap) should not exceed recommended Tc values. Exceeding that temperature may degrade the device characteristics or may even damage the device.

All reflow activities were performed in a belt oven with an inert atmosphere (Nitrogen - N2). During calibration, the zone temperature and belt speed are varied and the temperature of the device temperature monitored and compared to the JEDEC recommendations (Table 5 and Figure 31) and solder paste supplier recommendations.

Long preheat or soaking time will allow flux to outgas properly and may help minimize the solder voids of a typical Pb-free solder paste.

Table 5. SAC Reflow profile classification (JEDEC J-STD-020)

Profile Feature	Pb free Assembly (SAC alloys)
Preheat Soak • Temperature Min (Ts_{min}) • Temperature Max (Ts_{max}) • Time (Ts_{min} to Ts_{max}) (ts)	 • 150 ºC • 200 ºC • 60 – 120 seconds
Ramp-up rate (T_L to T_P)	3 ºC/second max
Time 25 ºC to Peak Temperature (Device supplier Maximum)	8 minutes max
• Liquidus temperature (T_L) • Time maintained above Liquidus temperature (t_L)	• 217 ºC • 60-150 seconds
Time (t_p) within 5 ºC of the specified (T_c).	30 seconds
Ramp-down Rate (T_P to T_L)	6 ºC/seconds max

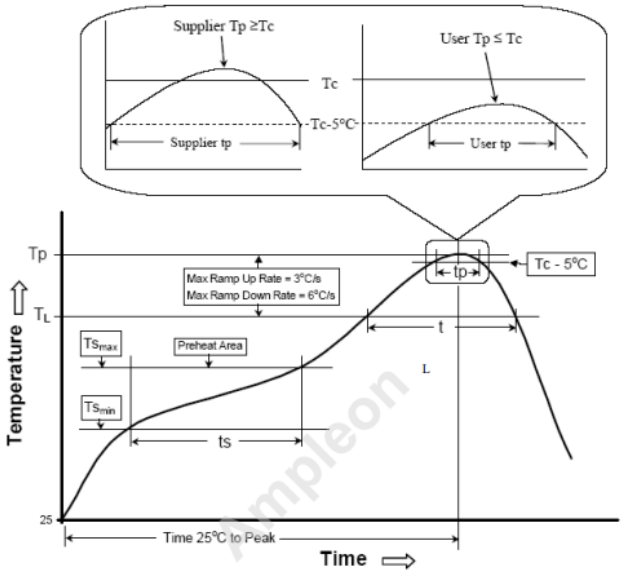

Figure 31. Classification profile based on JEDEC (JEDEC J-STD-020)

7. Inspection

Non-destructive vision/optical inspection methods are preferred to verify soldering quality.

Common methods for design and process development purposes are:

- Manual or automatic optical inspection.
- Examination by X-ray.
- SAM (Scanning Acoustic Microscope).
- Cross-sectional analysis.
- Dye penetration test.

7.1 Optical inspection

Easiest method for solder joint inspection is through optical inspection to look for solder joint profile and visual defects like shorts, misalignment.

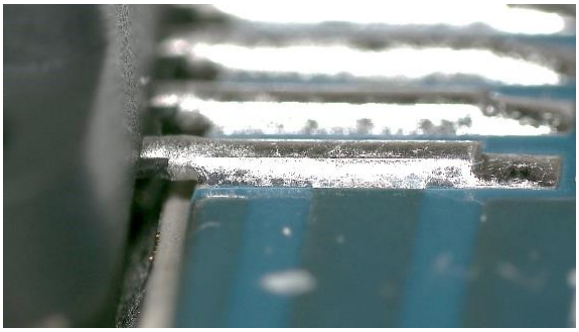

Figure 32. Visual appearance straight leads device

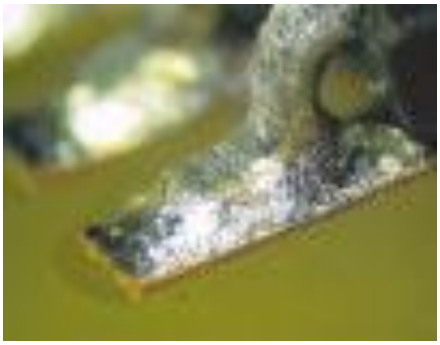

Figure 33. Visual appearance gullwing device

7.2 X-ray inspection

It's an efficient inline control to detect soldering defects such as poor soldering, bridging, voiding and missing parts. Some defects such as broken solder joints are not easily detectable by X-ray.

Void levels do provide confidence in the materials and soldering process.

Figure 34 shows typical X-ray photographs of an overmold package.

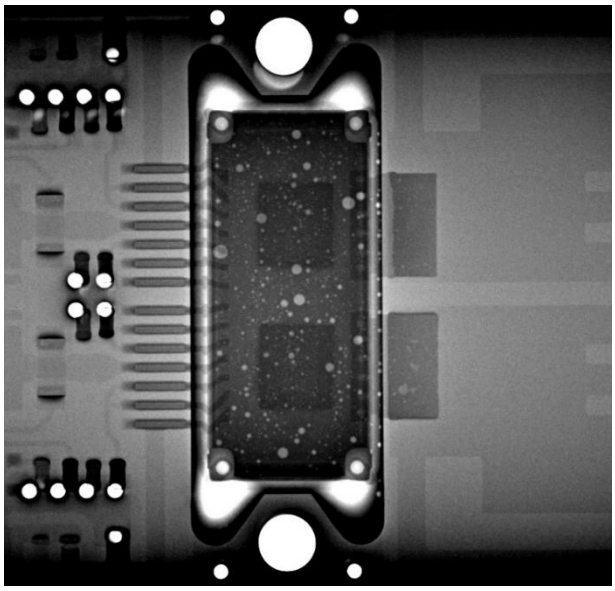

Figure 34. X-ray of a soldered device

Generally, the extent of voiding depends on the board pad size, the stencil layout, the solder paste, the reflow profile, the via layout and solderability of PCB/package.

General considerations to minimize X-ray impact to the electrical performance of semiconductor ICs are provided in Appendix 9.3 of this document.

7.3 SAM (Scanning Acoustic Microscope)

This method is used to examine in particular the interface between the exposed heat spreader/flange and the heat sink, as it is not easily detectable by X-ray. Variability in gray scale (dark – bright) indicates presence of voids.

The solder interface between the flange and heat sink have been inspected as shown in Figure 35. This provides information on the quality of the soldered interface (based on the level of voids). This technique can also be applied to assess the soldering quality of the leads to the PCB.

The introduction of finished PCBs into a DI water bath is considered a reliability risk, if parts will be used after SAM, dry bake should be performed, 8 hours at 125°C (typical conditions may differ depending on application).

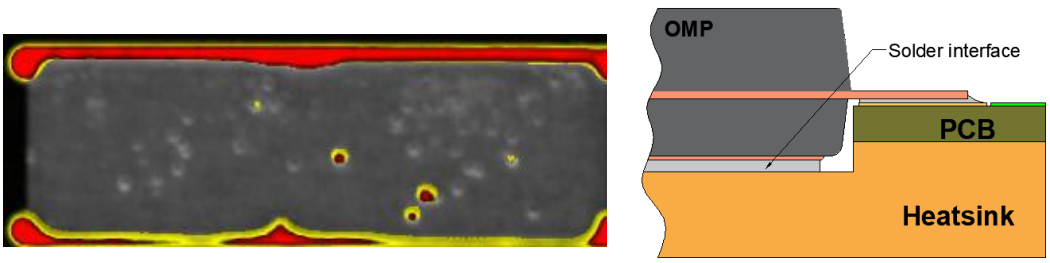

Figure 35. SAM of soldered interface between flange & heat sink

7.4 Cross-sectional analysis

Cross-sectioning can offer detailed information about the solder joint quality.

Since it's a destructive method, cross-sectioning during monitoring is naturally not practical and it's indicated for development and failure analysis.

Figure 36 shows typical cross section of LGA component.

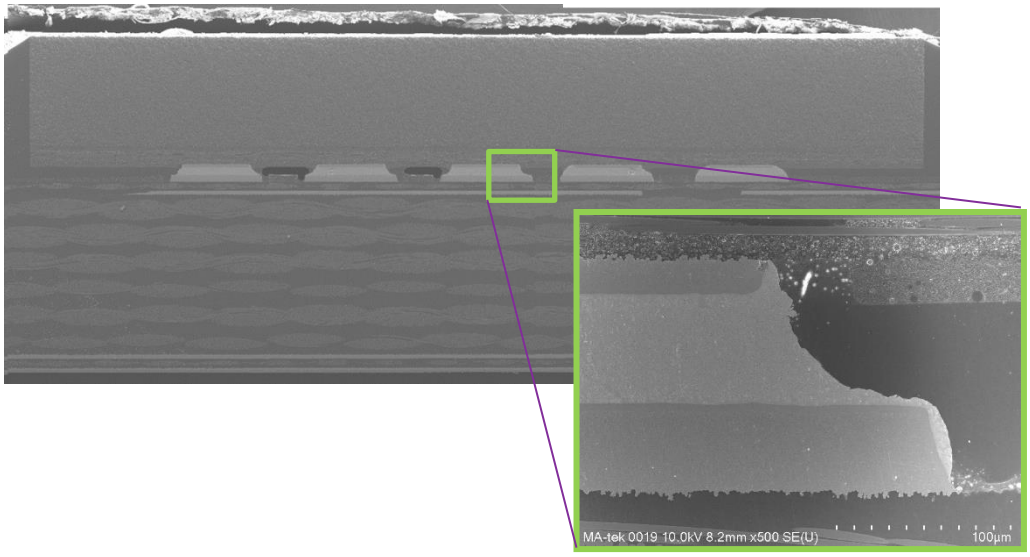

Figure 36. LGA cross section

8. Reworking

Although repair of solder joints is generally possible, it can be challenging and require proper optimization. Difficulty will vary depending on package type and PCB design.

A package lead or a land pad in case of a leadless package not soldered properly may be repaired by heating it with the tip of a soldering iron. In that case, it is sufficient to heat the lead/pad until the solder melts completely, and a new device should not be necessary.

The soldering iron temperature must be set such that the package surface temperature doesn't exceed its maximum allowed temperature. Soldering iron should also be ESD compliant.

In other situations, if a defective component is observed after board assembly, there may be a need to replace the package. In that case, the rework process should consist of the following steps:

- Removal of old package.
- Site preparation.
- Solder application.
- New package placement.
- Soldering new package.

8.1 Removal of the package

It is recommended to use rework station with a hot plate combined with hot air heat transfer (Figure 37 – setup for bottom and top heating).

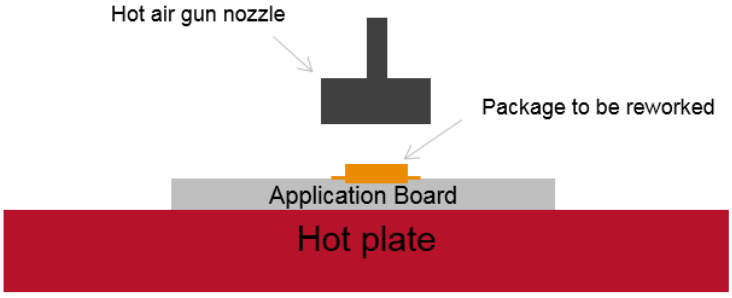

Figure 37. Setup schematic – package removal

Rework station equipment should be able to control:

- Temperature and time for bottom heating.
- Temperature, time, distance and air flow for top heating.
- Temperature profile should be adaptable to different packages sizes and thermal masses.
- Ensure that the peak temperature and temperature ramps are according with the standard reflow process.

- High mechanical forces shouldn't be applied to remove or move component, this can compromise future failure analysis on the component or/and PCB. It is recommended to use vacuum pipette (ESD safe).

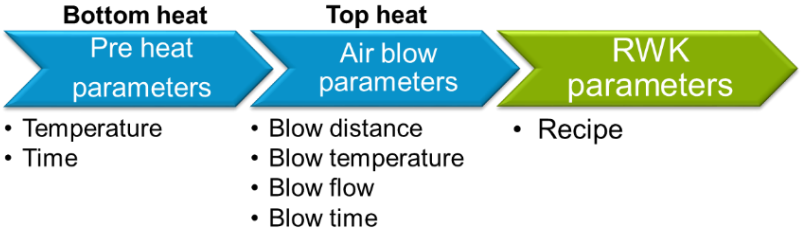

Figure 38. Key rework station parameters

The process steps are as follows:

- Dry-bake (remove moisture from the PCB) for 8 hours at 125°C (typical conditions, may differ depending on application).
- Pre heat (uniform temperature in board) on hotplate with a temperature of 125°C (typical conditions, may differ depending on application).
- Reflow component to rework using the hot air. The Nozzle size and heat flow should be optimized to keep heat flow localized and still allow the melting of the solder on the component.
- Package removal: as soon as the solder melts, lift the package off the PCB using a vacuum nozzle. Do not lift the package before the solder in the joints has melted completely, as this may damage the package and the PCB.

Throughout this process, care must be taken that there are no contacts with neighboring components.

8.2 Site preparation

After the package has been removed, the PCB pads must be prepared for the new package. Prepare the pads by removing any excess solder and/or flux remains. Ideally this is done on an appropriate de-soldering station. Alternately, use a soldering iron set to the temperature specified for the solder that was originally used to attach the package. Clean the pads using the soldering iron and solder wick, or another in-house technique. Note: use a temperature that is needed to just liquefy the solder but that does not damage the PCB.

After most of the solder has been removed from a solder land, a very thin layer of solder will be left, on top of a few intermetallic layers. In the case of Cu pads, for example, there will be layers of Cu_3Sn, Cu_6Sn_5, and finally solder, on top of the Cu. The top layer of solder is easily solderable.

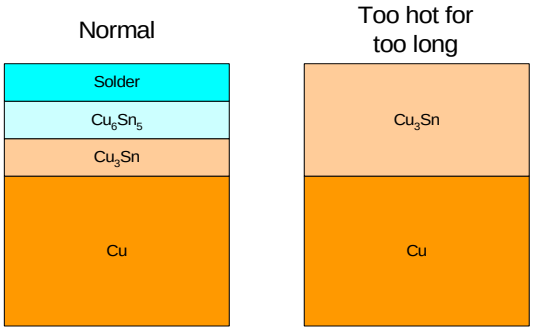

Figure 39. Overheating and Cu_3Sn formation

If, however, the pad is heated too much during removal of the rejected IC package, and during site preparation, the top two layers will also be converted into Cu_3Sn (Figure 39), in that case, there will only be the Cu_3Sn inter-metallic layer on top of the Cu. Unfortunately, Cu_3Sn is hardly wettable. As a result, it will become very difficult to solder the replacement package at this location. Therefore, care must be taken during reject package removal and site redress, that the solder lands are heated only as much as is absolutely necessary.

8.3 Solder application

A mini stencil is preferable method to apply solder.

Stencil should have same design as the stencil used in normal assembly of the component (thickness, apertures, pattern).

In case space constrains due to other components nearby and mini stencil cannot be used, solder paste dispense method can be used. Make sure that solder volume is consistent across all packages leads/pads.

After solder application solder volume must be visually controlled.

8.4 Placement of the new package

Mount a new package in much the same way as the original package was mounted. Re-use of removed packages is not recommended.

In case manual mounting, use a good optical system (e.g. microscope with min 25x magnification) for placement and alignment of package.

8.5 Soldering of the new package

New package should be soldered to the PCB in the same manner as the original package.

In case reflow furnace is not possible, same method as used for the package removal can be used (hot plate combined with hot air nozzle), heating/cooling profile should have ramp rates and peak temperatures similar to the initial reflow.

9. Appendices

9.1 MSL

MSL (Moisture Sensitivity Level).
If there is moisture trapped inside a plastic over molded surface mount package, and the package is exposed to a reflow temperature profile, the moisture may turn into steam, which expands rapidly. This may cause damage to the inside of the package (delamination), and it may result in a cracked semiconductor package body (the popcorn effect). A package's MSL, depends on the package characteristics and on the temperature it is exposed to during reflow soldering.

MSL level are determined according JEDEC standard J-STD-020 [1]. Depending on the damage after this test, an MSL of 1 (not sensitive to moisture) to 6 (very sensitive to moisture) is attached to the semiconductor package. For every plastic over molded product, this MSL is given on a packing label on the shipping box. An example of a packing label is given in Figure 40.

Figure 40. Example of MSL information on packing label

An MSL corresponds to a certain out-of-bag time (or floor life). If semiconductor packages are removed from their sealed dry-bags and not soldered within their out-of-bag time, they must be baked prior to reflow, to remove any moisture that might have soaked into the package. MSLs and temperatures on the packing labels are always to be respected. Naturally, this also means that semiconductor packages with a critical MSL may not remain on the placement machine between assembly runs. Nor should partial assembled boards, between two reflow steps, be stored longer than indicated by the MSL level.

The semiconductor package floor life depends on the MSL level and should be accordance to the J-STD-020.

9.2 ESD

Damage to semiconductors from Electro Static Discharge (ESD) is a major cause of rejects and poses an increased risk to miniaturized packages. Electrostatic charge can be stored in many things, for example, fiber clothing, moving machinery, objects with air blowing across them, plastic storage bins, sheets of paper stored in plastic envelopes, paper from electrostatic copying machines, and people. Electrostatic discharge is the transfer of an electrostatic charge between bodies at different potentials and occurs with direct contact or when induced by an electrostatic field. Generally, ESD devices are marked with warning sign as in Figure 41.

Figure 41. ESD warning signal.

9.2.1 Workstations for handling ESD sensitive components

Figure 42 shows a working area suitable for safely handling electrostatic-sensitive devices. The following precautions should be observed:

- Workbench and floor surface should be lined with anti-static material.
- Persons at a workbench should be earthed via a wrist strap and a resistor.
- All mains-powered equipment should be connected to the mains via an earth leakage switch.
- Equipment cases should be grounded.
- Relative humidity should be maintained between 40 % and 50 %.
- An ionizer should be used to neutralize objects with immobile static charges in case other solutions fail.
- Keep static materials, such as plastic envelopes and plastic trays away from the workbench. If there are any such static materials on the workbench remove them before handling the semiconductor devices.
- Refer to the current version of the handbook EN 100015 (CECC 00015)[3] “Protection of Electrostatic Sensitive Devices” (see 11), which explains in more detail how to arrange an ESD protective area for handling ESD sensitive devices.

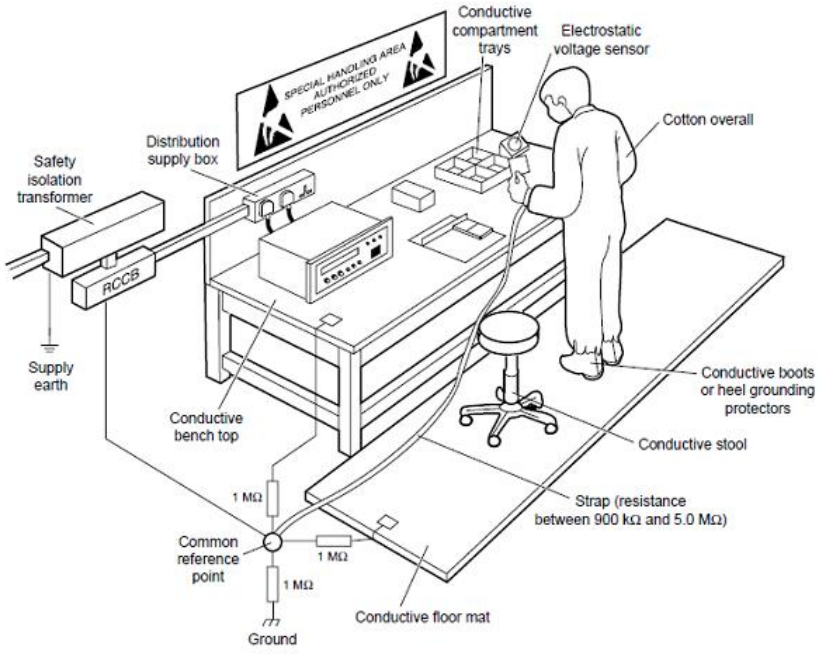

Figure 42. Example of a work station

9.2.2 Receipt and storage of components

Packing for electrostatic devices should be made of anti-static/conductive materials.

Warning labels on both primary and secondary packing show that the contents are sensitive to electrostatic discharge. The electronic components should be kept in their original packing whilst in storage. If a bulk container is partially unpacked, the unpacking should be done at a protected workstation. Any electronic components that are stored temporarily should be re-packed in conductive or anti-static packing or carriers.

9.2.3 PCB assembly

All tools used during assembly, including soldering tools and solder baths, must be grounded. All hand tools should be of conductive or anti-static material and where possible should not be insulated. Standard precautions for manual handling of electrostatic-sensitive devices need to be followed.

9.3 X-ray considerations

X-ray can affect the electrical performance of semiconductor ICs, a phenomenon documented in scientific literature. X-ray tool vendors provide application notes on methods to minimize X-ray impact on semiconductors. Customers are strongly advised to consult their X-ray tool vendor for specific guidance, as the impact depends on various factors such as spectrum, filters, collimators, and software settings.

General considerations to minimize X-ray impact:

- Minimize the total X-ray dose. Ampleon has conducted X-ray inspection to verify good soldering on a board. This can be achieved with a dose << 1 Gy. A maximum dose of <<1 Gy is recommended including rework. Maximum dose depends on the x-ray spectrum. Internal evaluations by Ampleon have shown that the dose needed to make sharp pictures has a negligible effect on the electrical characteristics of its products. However, these findings are for reference only and do not constitute a warranty or guarantee.
- Use collimators to reduce secondary exposure.
- Apply filters to minimize the softer part of the X-ray spectrum, which has the most significant impact.
- Regularly monitor the X-ray dose to prevent overexposure due to tool malfunction.
- Inspect the device from the back, allowing the application board and/or flange or lead frame to absorb a significant part of the X-ray radiation.
- Assess potential electrical performance shifts caused by X-ray exposure to verify the product performance remains within specified limits. Special attention should be given to Idq (quiescent current), caused by a shift in Vt (threshold voltage). X-ray can lead to a Vt shift caused by charging of the gate oxide in LDMOS devices. These charges can be released during lifetime. The shift in Idq caused by X-ray needs to be well within the requirements from application perspective.

10. Abbreviations

Table 6. Abbreviations

Acronym	Description
AOI	Automatic optical inspection
DFN	Dual Flat pack No leads
ENEPIG	Electroless Nickel, Electroless Palladium, Immersion Gold
HVSON	Thermal enhanced very thin small outline; no leads
LGA	Land Grid Array
MSL	Moisture Sensitivity Level
MTTF	Mean Time To Failure
NSMDP	Non-Solder Mask Defined Pads
OMP (packages)	Over-Molded Plastic
OSP	Organic Solderability Preservative
PA	Power Amplifier
PCB	Printed Circuit Board
PQFN	Power Quad Flat No-Leads
Ra	Average Roughness
RF	Radio Frequency
RH	Relative Humidity
SAC (solder)	Sn (Tin) Ag (Silver) Cu (Copper)
SMDP	Solder Mask Defined Pads
SnPb (solder)	Sn (Tin) Pb (Lead)
TO	Transistor Outline

11. References

[1] IPC/JEDEC J-STD-020

Joint IPC/JEDEC Standard for Moisture/Reflow, Sensitivity Classification for Non hermetic Surface Mount Devices

[2] IPC-7351

Generic requirements for Surface Mount Design and Land Pattern Standard, IPC

[3] EN 100015/CECC 00015

Protection of Electrostatic Sensitive Devices, European Standard

[4] 3997.750.04888

Quality reference handbook, Ampleon

[5] IPC-A-610

Acceptability of Electronic Assemblies, IPC

[6] MIL-STD-883

Test Methods standard microcircuit

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